Friden, Inc.

ELECTRONIC CALCULATOR 130

SERVICE MANUAL

TP-158SL-1

Friden, Inc.
SAN LEANDRO · CALIFORNIA
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FRIDEN ELECTRONIC CALCULATORS

EC-130 SERVICE MANUAL

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SECTION 1 - GENERAL DESCRIPTION

A. SCOPE OF MANUAL

This manual covers the maintenance of the EC-130 (Figure 1-1). The maintenance of the EC-130 requires extensive and thorough knowledge of the machine, especially as to logic functions. While most troubles are of a component failure nature, localization of the trouble to a particular component may involve extensive tracing of logic signals through the plug in circuit cards.

Since the EC-130 uses dynamic storage, and the logic actions are predicated upon time through the timing chain and Entry Phase Counter, knowledge of machine timing and proper use of a Tektronix 535 Oscilloscope (or equivalent) is necessary.

B. ELECTRICAL CHARACTERISTICS

The EC-130 operates on 115V ±10% AC, 50-60 cycles, and may be connected to any standard AC outlet. Specially designated machines for export only are designed for operation at 220 VAC.

The EC-130 is fused internally with a 1 Ampere line fuse and a 2 Ampere fuse in the -12 VDC power supply output.

C. PHYSICAL CHARACTERISTICS

The EC-130 is 22" long, 18" wide, 10" high, and weighs approximately 45 lbs. The relatively small size of the EC-130 makes it suitable for placement on any standard office desk, and the light weight makes it truly portable.

D. OPERATIONAL DESCRIPTION

The operation of the EC-130 is controlled by an ON-OFF switch lever located on the lower front right-hand side. Once the lever has been placed to ON position and the display appears on the CRT, the EC-130 is ready for keyboard control.

1. DISPLAY

The display on the EC-130 consists of four 13-digit registers, each with an algebraic sign column. No sign displayed means a positive number in that register. If the number is negative, a minus sign is displayed in the extreme right-hand position of the register.

The EC-130 employs a new concept in computation which permits storage of intermediate answers for later use according to the requirements of the problem being solved. The four registers are specified and arranged in a particular manner. (See Figure 1-1.)

a. REGISTER #1. The lowermost register is designated as Register 1, also known as the "Answer Register". All numbers enter the display through this register, and are displaced upward by subsequent entries. At the finish of any arithmetic function, the answer to the computation appears in Register 1. This register is also brightened with respect to the other registers.

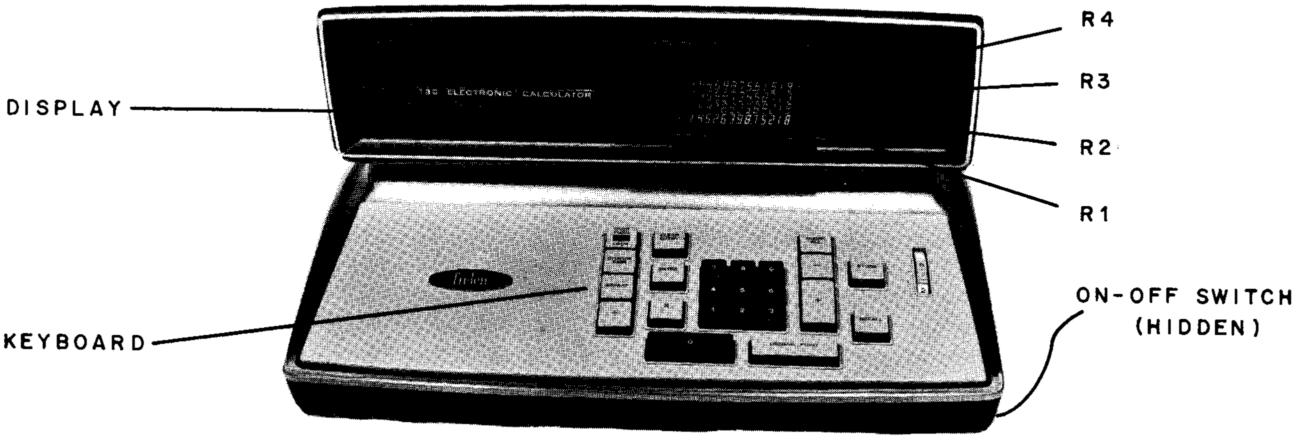


Figure 1-1. Electronic Calculator 130

b. REGISTER #2. One of the numbers of an arithmetic operation is in this register; the other number is in Register 1. When the numbers in these registers are used in an arithmetic operation, the answer appears in Register 1, and the numbers in Register 3 and 4 are automatically shifted down by one register.

c. REGISTERS #3 AND #4. These registers are used for storage of numbers, or intermediate answers. When the lower two registers are used for computation, these registers shift down one register with the previous Register 3 number being placed in Register 2 and immediately available for further computation. If Register 1 is used for an entry (or Recall, or Repeat) when all registers already contain numbers, the contents of Register 4 shift up and are effectively discarded, or lost.

2. KEYBOARD

The keyboard (Figure 1-2) is the only mechanical portion of the EC-130. When a key is pressed, the mechanical motion of the key is translated into the closing of one or more switches that initiate the electronic action of the machine.

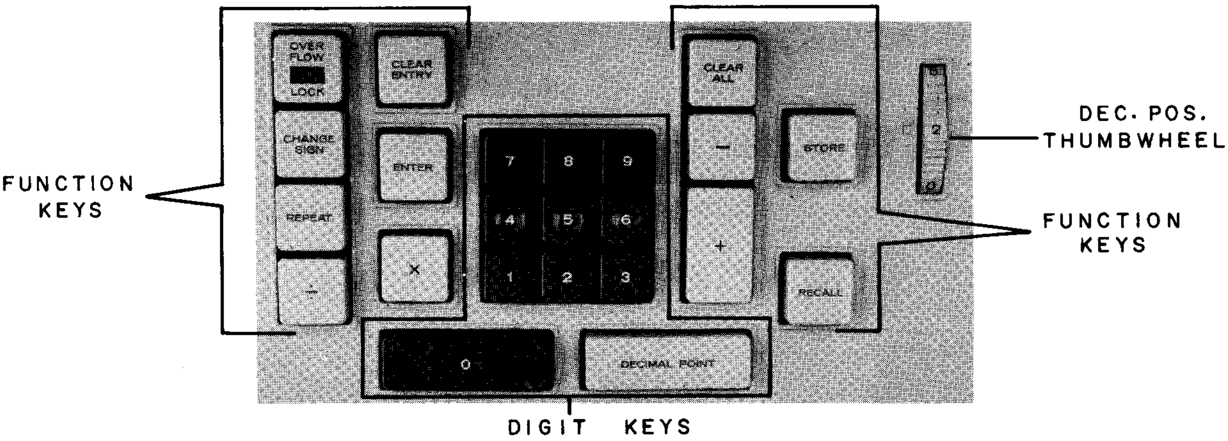


Figure 1-2. Keyboard Arrangement

a. DIGIT KEYS. On the keyboard are 10 digit keys (0 - 9) and a decimal point key that enable entering numbers in the machine. As a number is entered in the machine by sequential depression of the digit keys, that number appears digit by digit in Register 1, but without the decimal point.

The completion of a number entry is signified in the machine by pressing ENTER key, which then decimal aligns the entered number. Initiation of any function also aligns the number in Register 1, if not already aligned. Therefore, ENTER key need not be used except in the entering of more than one number with no other functions being performed between the number entries.

DECIMAL POINT key is used when entering a number containing a decimal. If DECIMAL POINT key is not used, the number is sensed as a whole number and decimal aligned to the left of the decimal point.

An automatic "Decimal Interlock" feature is provided that prevents entering more decimal digits than can be accomodated after decimal alignment. Assume a decimal point position set at 2, then only two digits to the right of the decimal point can be utilized. The third and subsequent digits entered after DECIMAL POINT key is pressed are automatically disregarded.

b. FUNCTION KEYS. The function keys are designated as those keys that rearrange the data on display, or initiate arithmetic operations upon the data in Registers 1 and 2.

(1) ENTER - The ENTER key completes a number entry by decimal aligning Register 1.

(2) STORE - The STORE key places the number in Register 1 into an undisplayed storage register. Once the number is stored it can be recalled as often as desired but is not changed except by replacement with a new number, or by pressing CLEAR ALL key, which removes all data.

(3) RECALL - The RECALL key duplicates in Register 1 the number that is in the storage register.

(4) REPEAT - The REPEAT key duplicates in Register 2 the number that is in Register 1.

(5) ADD (+) - The Add key initiates machine action that results in the numerical addition of the numbers in Register 1 and Register 2, with the result (answer) appearing in Register 1. When the answer appears in Register 1, numbers in Registers 3 and 4 are displayed as shifted down by one register.

(6) SUBTRACT (-) - The Subtract key initiates machine action that results in the numerical subtraction of the number in Register 1 from the number in Register 2, with the answer appearing in Register 1 and numbers in Registers 3 and 4 shifting down. If the number in Register 1 is larger than the number in Register 2, the subtraction still takes place. However, before display, the numerical result is complemented and then displayed with the sign changed.

(7) MULTIPLY (X) - The Multiply key initiates machine action that results in the numerical multiplication of the number in Register 1 by the number in Register 2 with the answer appearing in Register 1, and the numbers in Registers 3 and 4 shifting down.

(8) DIVIDE (÷) - The Divide key initiates machine action that results in the numerical division of the number in Register 2 by the number in Register 1, with the answer appearing in Register 1 and the numbers in Registers 3 and 4 shifting down by one register.

c. ADDITIONAL KEYS. In addition to the digit keys and function keys are keys that initiate machine operations such as clearing Register 1, clearing all data, etc.

(1) CLEAR ENTRY - The CLEAR ENTRY key initiates machine action that results in the removal of the number in Register 1, usually in the case of a mistake being made during a number entry.

(2) CLEAR ALL - The CLEAR ALL key initiates machine action that results in the removal of all numbers from the machine. This includes any number in storage, as well as on the display.

If the machine is turned off, or power to the machine is interrupted for any reason, this also results in the removal of all data.

(3) CHANGE SIGN - The CHANGE SIGN key initiates machine action that results in changing the sign of the number in Register 1. When a number is entered, it is sensed as a positive number. Certain mathematical operations involve the use of negative numbers, and the Change Sign function enables the number to be made negative after the number is entered. The CHANGE SIGN key also enables the sign of the number in Register 1 to be reversed at any desired point during a complex mathematical operation.

(4) OVERFLOW LOCK - If a number that is entered, or an answer developed, contains more whole number digits than there are columns to the left of the decimal point when the number is decimal aligned by ENTER key or during a function, OVERFLOW LOCK lights up and the keyboard locks-up, which designates an entry, or an answer, larger than machine capacity.

The overflow condition can be cleared by any one of three keys: CLEAR ENTRY, CLEAR ALL, or OVERFLOW LOCK. CLEAR ENTRY removes the overflow by removing the number in Register 1, which is the entry, or answer, that caused the overflow. CLEAR ALL removes the overflow by clearing all numbers from the machine, which includes the entry, or answer, that caused the overflow. OVERFLOW LOCK removes the keyboard lock-up without clearing any numbers, which leaves a portion of the entry or the answer displayed in Register 1.

E. DECIMAL POINT SELECTOR

On the right-hand side of the keyboard is a thumb-wheel which permits selection of the column position of the decimal point. There are five positions available: 0 - 2 - 5 - 7 - 13. A field option is available that changes position 7 to position 9.

Once the decimal position is chosen with this wheel, automatic decimal alignment of all entries and answers takes place with respect to this position.

F. SERVICE CALLS

Many of the repairs and adjustments to the EC-130 are accomplished in the customer's office. Following are certain servicing procedures that may prove useful, not only to the beginning technician but also to the more experienced.

1. CUSTOMER CONTACT

A Service Technician is probably the most often seen representative of the Company, especially at the office "working" level as distinguished from "management". As such, it is important that the technician be neat, well-groomed, and courteous.

Competition is keen in the office equipment field. Often, the choice between competing machines is the service factor. As a part of the service organization, the service technician is an important representative and should look, act, and conduct himself as such. It is not enough just to be a good technician; to know the machine; or to be able to adjust the machine satisfactorily. It is also very important to leave the customer satisfied, not only that the machine is working well, but also that he has been treated with respect; his wishes have been courteously received and complied with to the maximum practical extent; and that the whole servicing procedure was conducted by a neat, efficient, courteous, and well-trained representative.

As a part of customer contact, the technician must find out, as courteously and expeditiously as possible, the cause of customer complaint. Very often, courteous listening to the machine operator, even if not directly applicable to machine malfunction, will leave a very good impression. The first step in service procedure is to find out what is wrong from the standpoint of the customer.

2. MACHINE CHECKOUT

Machine checkout is a series of semi-standardized steps used in determining a machine malfunction. Necessarily, experience with the EC-130 will enable each service technician to develop his own checkout procedures. The following is a guide to be used if desired.

a. AC POWER. Since the EC-130 is an electronic machine, it must be furnished with AC power at 115V, 50-60 cycles from a convenient 3-wire, grounded, AC outlet. One of the first steps in a checkout is to determine if power is being furnished to the machine, especially if the preliminary inspection reveals a blank display.

On the right hand side of the machine, beneath the top cover, are two fuses. The best check of the fuses is to replace them with two known good fuses of the same type and current rating.

On the bottom front right side of the machine is an On-Off switch. To turn on the machine, this switch is placed forward. The On-Off switch is interlocked with the right hand top-cover holding screw. (See Top Cover Removal and Replacement Procedure.)

b. VISUAL INSPECTION. Visual inspection of the display can reveal malfunctions such as character malformation, displacement, and abnormal height or width. There are two purposes in the design of the display. One is to provide a means of visually checking the numbers to be operated with, and the second is to provide a clear and pleasing visual presentation. Certain aspects of the visual presentation are adjustable to customer satisfaction if desired. Visual display adjustments are covered in Section 3 of this manual.

c. STANDARD PROBLEM. Following is a standard problem that will check most of the functions of the EC-130; Decimal Point Selector on 0:

(1) Press CLEAR ALL
(2) Press digit 1-1-1-1-1-1-1
(3) Press ENTER
(4) Press STORE
(5) Press RECALL
(6) Press REPEAT
(7) Press Multiply (X)

Register one shows: 1 2 3 4 5 6 7 6 5 4 3 2 1
Enter, Store, Recall, Repeat, and Multiply are checked in the above procedure.

(8) Press RECALL
(9) Press Divide (÷)

Register one shows: 0 0 0 0 0 0 1 1 1 1 1 1 1
Divide is checked.

(10) Press REPEAT
(11) Press Add (+)

Register one shows: 0 0 0 0 0 0 2 2 2 2 2 2 2
Add is checked.

(12) Press RECALL
(13) Press Subtract (-)

Register one shows: 0 0 0 0 0 0 1 1 1 1 1 1 1
Subtract is checked.

(14) Press "0"
(15) Press Divide (÷)

Display remains blanked.
Unsolvable problem, answer would be infinity.

(16) Press CLEAR ALL
(17) Move Decimal Point Locator to 7 on dial.
(18) Press digit: 1-1-1-1-1-1-1
(19) Press ENTER

OVERFLOW LOCK lights, keyboard locks-up. Entering of too many whole number digits is checked.

(20) Press CLEAR ENTRY
(21) Move Decimal Point Locator to 2 on dial.
(22) Press digit: 1-1-DECIMAL POINT-1-1-1
(23) Press ENTER

Register one shows: 00000000011.11
Entering of too many decimal digits is checked.

G. SERVICING DOCUMENTATION

In addition to the Service Manual are other documentary aids to servicing of the EC-130. They are listed and briefly explained as follows:

1. COMPUTER PRINTOUT (MDD)

The computer printout is the basic engineering documentation of the EC-130. This type of documentation will also be used for later machines in the design progression. As such, it contains authoritative information in a concise form that lends itself easily to changes, extraction of production information, part number and location information, and a coherent method of logic analysis by use of a specialized logic equation format.

a. BASIC MDD. The Computer Printout (MDD), as reproduced for service use, contains four parts: Glossary of Terms, Logic Equations, Construction File, and Schematic Diagrams.

(1) Glossary of Terms. The glossary lists in alphabetical order all of the logic terms used in the logic equations. The glossary further provides the number of the equation that produces the term, a list of equations that contain this term, and a brief description of the term.

(2) Logic Equations. The equations section contains the logic that produces each listed term in the glossary. The equations are written in a specialized form called "Modified Polish Notation". The equations section also contains location information in a visual coordinate system that permits the location of a signal reference point for any of the logic terms or gates referenced in a particular equation.

(3) Construction File. The construction file contains production information useful in providing drilling coordinates, insertion coordinates, lead orientation, etc. The main use of the construction file is to provide the service technician with component information on each element that makes up the logic, especially the part number of the component parts.

(4) Schematic Diagrams. Certain analog circuits such as the Power Supplies, Display Deflection Circuits, etc. do not lend themselves easily to logic equation form or coordinate component location. Therefore, these circuits are furnished in schematic diagram form. The schematic section also contains wire lists, visual X-Y coordinate card pictures, and other information of use to the servicing technician.

2. LOGIC BLOCK DIAGRAM

To aid in the training of technicians and the servicing of the EC-130, a Logic Block Diagram has been evolved from the information contained in the Computer Printout.

The Logic Block Diagram contains the logic of the EC-130 in the form of gates, inverters, FF's, and other elements. The layout of the Logic Block is primarily designed for ease of training, but is also extremely useful in servicing.

The Logic Block Diagram also contains visual coordinate information to enable a servicing technician to trace a logic fault back to an originating element by means of an oscilloscope in a rapid, time-saving manner.

3. ENGINEERING DRAWINGS

The production of the EC-130 necessitates engineering drawings regarding assembly, component layout, etc. Such of these drawings as are thought useful in servicing are available as requested. Usually, the engineering information is furnished to the technician by means of parts lists, service letters, and service correlation of engineering drawings.

4. SERVICE LETTERS

In the event that it is desired to get an engineering change into the field documentation immediately, a Service Letter is prepared containing all pertinent information.

The Service Letter is also used to convey special repair techniques, common trouble notes, and other servicing information of value to the technician.

The Service Letter file should be well kept and each technician should be thoroughly familiar with the contents.

H. SERVICE RECORDS

The Procedures Manual contains the latest promulgated method for handling specific service records, and other service office documents. However, the ordering of service documentation is an area of special attention.

To order an engineering drawing, the engineering number of the drawing must be given. To order a service produced document, the service numbering system must be used. For example, on each reproduceable page sized drawing in the Service Manual is a number such as D-130-82T. To order a drawing, this number is used.

Drawing Number Format:

D - Designates a drawing; A "P" would designate a photograph.
130 - Model Number.
82 - Identification number in a series of numbers.
T - Information and format developed by Technical Servicing Group at Home Office. An "E" would designate an engineering drawing which has been redrawn by service. A "W" would designate a drawing which was originated by the Technical Writing Section for use in a manual.

In the event that a photograph, or less-than-page sized drawing appearing in a manual is desired, reference to the manual section and page is sufficient.

SECTION 2 - ANALYSIS OF OPERATION

A. FUNCTIONAL DESCRIPTION

The functional description of the EC-130 is a brief explanation of the major functional circuits on a block diagram level, with reference to the Overall Block diagram, Figure 2-1.

(NOTE: Figures not in chronological order with the text are Foldouts and will be found at the end of this section.)

1. DATA ORGANIZATION

The data is organized in the machine by the action of timing signals on the counters. The action of the counters controls the placement of data on the delay line, and on the CRT display. The CRT displays data in a specific pattern (See Figure 2-2).

Some of the data relationships in the machine are not displayed but are used for necessary arithmetical, storage, or timing operations. The major time relationships in the machine are: Bit time, Register time, Column time, and Word time.

a. BIT TIME. Each R time is composed of sixteen (16) Bit (B) times, of which nine (9) are used for pulses that represent digits. One B time is equal to 3 μsec.

b. REGISTER TIME. There are six register (R) times, of which four are displayed (See Figure 2-3). Each R time is equal to 48 μsec. Each register time can contain one digit of a number.

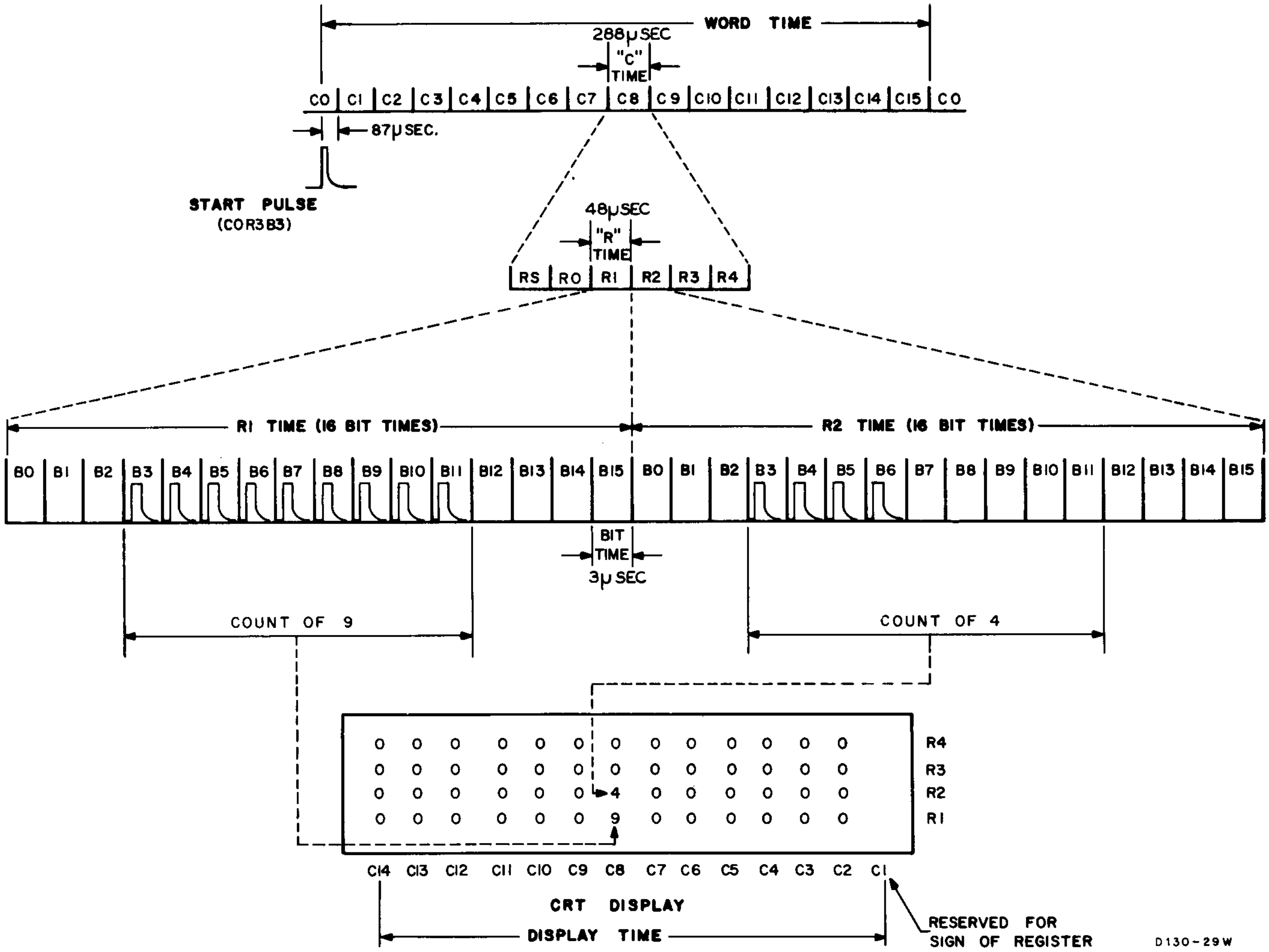

WORD TIME
288μSEC
"C" TIME
C0 C1 C2 C3 C4 C5 C6 C7 C8 C9 C10 C11 C12 C13 C14 C15 C0
87μSEC.
START PULSE
(COR3B3)
48μSEC
"R" TIME
RS R0 R1 R2 R3 R4
R1 TIME (16 BIT TIMES)
R2 TIME (16 BIT TIMES)
B0 B1 B2 B3 B4 B5 B6 B7 B8 B9 B10 B11 B12 B13 B14 B15
B0 B1 B2 B3 B4 B5 B6 B7 B8 B9 B10 B11 B12 B13 B14 B15
BIT TIME
3μSEC
COUNT OF 9
COUNT OF 4
4
9
R4
R3
R2
R1
C14 C13 C12 C11 C10 C9 C8 C7 C6 C5 C4 C3 C2 C1
CRT DISPLAY
DISPLAY TIME
RESERVED FOR SIGN OF REGISTER
D130-29W

Figure 2-2. Data Organization

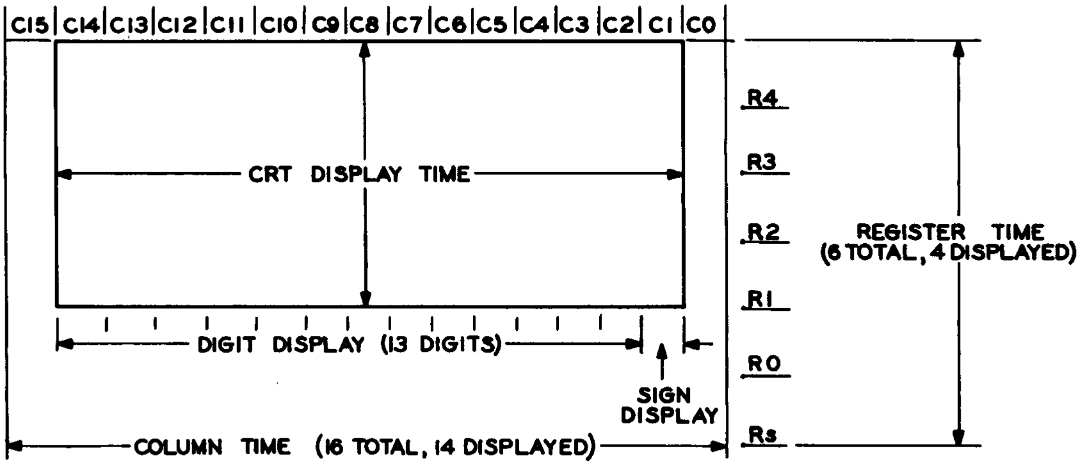

C15
C14
C13
C12
C11
C10
C9
C8
C7
C6
C5
C4
C3
C2
C1
C0
CRT DISPLAY TIME
R4
R3
R2
R1
R0
Rs
REGISTER TIME (6 TOTAL, 4 DISPLAYED)
DIGIT DISPLAY (13 DIGITS)
SIGN DISPLAY
COLUMN TIME (16 TOTAL, 14 DISPLAYED)

Figure 2-3. Display Organization

c. COLUMN TIME. There are a total of sixteen (16) column (C) times, of which fourteen are displayed on the CRT. Each column time is equal to 288 μsec. One column (C1) is reserved for displaying the algebraic sign of the register. Columns two (C2) through fourteen (C14) display digits for each register. Thus, a total of thirteen (13) digits may be displayed in each register. Column fifteen (C15) is used in a divide operation, and column zero (C0) is not used.

d. WORD TIME. Word time is used to identify the total time available for a sequence of data. Word time consists of the six register times multiplied by fifteen column times.

2. BASIC TIMING

The organization of the data on the delay line, the positioning of the data on the display, and the sequence of internal machine operations are all related exactly by timing signals from the timing circuits (See Figure 2-4).

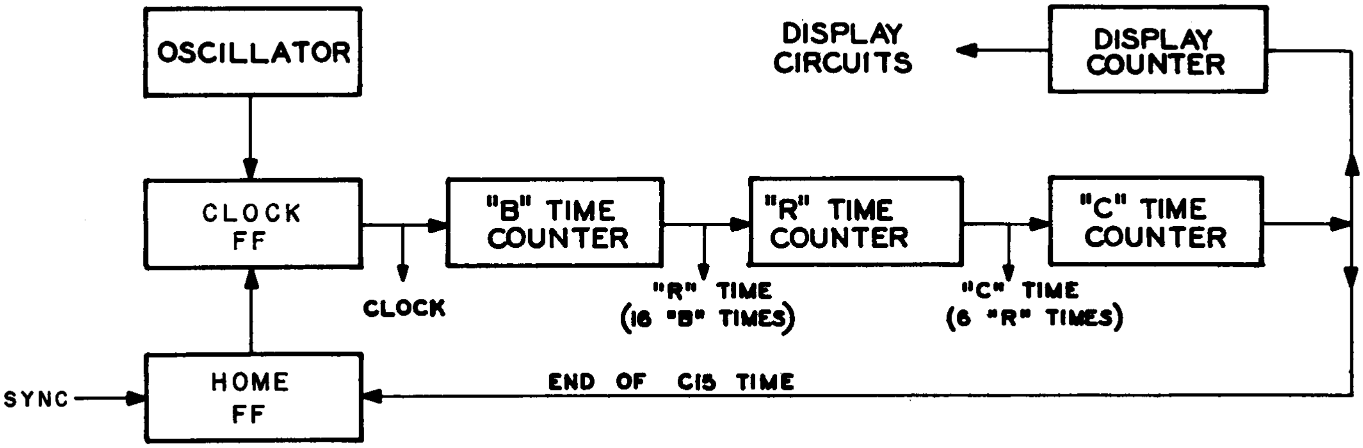


Figure 2-4. Timing Functional Diagram

a. SYNC PULSE. To maintain the relationship between the delay line and the timing circuits, the timing chain is stopped at the end of C15 time. This begins a period of time designated as "Home". When the machine is prepared for the entry of data after having first been turned on, or whenever all data has been cleared from the machine by CLEAR ALL key, a Sync pulse is placed on the delay line by the first function initiated by the keyboard. This Sync pulse is timed to occur before C1 time, and turns on the timing chain just before data is available at the output of the delay line. This ensures that the timing chain is always in step with the data, and thus the data can be identified correctly by timing chain signals.

b. CLOCK CONTROL. The basic time element is the frequency of the oscillator. The oscillator output drives the clock circuit, which puts out one pulse each Bit (B) time. While the oscillator runs continuously, the output of the clock is stopped at the end of C15 time. The clock is started again by the action of the Sync pulse at the time the first data is available at the output end of the delay line. This keeps the timing chain and the data synchronized so that the timing chain signals can be used to exactly identify the data by time as it comes off the delay line; and also while it is in the counter circuits.

3. TIMING CHAIN

The timing chain is a group of FF's that develop the basic time relationships in the machine. Timing signals from the timing chain enable the data to be organized in a specific sequence and arithmetical and data shifting operations to be performed at specified times that are time-related to the data sequence.

a. BIT TIME COUNTER. The B time counter circuits count the clock down by sixteen and provide an output pulse to the Register (R) time counter every sixteen (16) B times.

b. REGISTER TIME COUNTER. The R time counter circuits count down the output of the B time counter circuits by six, and provide an output pulse to the column (C) counter circuits every six (6) R times.

c. COLUMN TIME COUNTER. The column (C) time counter circuits count down the output of the R time counter circuits by 16, and provide an output pulse every sixteen (16) C times.

d. DISPLAY CONTROL COUNTER. The display counter provides signals to the display circuitry that enable each register to be displayed at the necessary time and proper position on the CRT. Register one (R1) is displayed twice for extra brightness and this is desirable, since the answer to an arithmetical operation always appears in this register.

4. COUNTER CIRCUITS

The counter circuits perform two functions: counting and shifting. Both are basic to machine operation. Counting means to progressively change the setting of a counter by the one-by-one addition of pulses, which is called "Serial Entry". There are two similar types of counters: Up Counter and Down Counter. They are capable of ten possible counts (settings).

a. UP COUNTER. The addition of a pulse to an up counter causes the setting to change in an upward direction from zero toward nine. Thus, one pulse into an up counter already set to three (3) results in a new setting representing four (4).

b. DOWN COUNTER. The addition of a pulse into a down counter will cause the setting to change in a downward direction from zero (representing 10) toward one. Thus, one pulse into a down counter already set to three (3) results in a new setting representing two (2).

5. DATA SHIFTING

Data shifting means to change the position of data with respect to time. To shift is to transfer the setting of one counter into another counter. Since the shift (transfer) of data is controlled with respect to time, the data can be moved with respect to time by shifting into specified counters.

Before explanation is made of the specific shifts used in machine operation, reference must be made to data organization with specific application to shifting.

a. DATA SEQUENCE. The data organization, called "data sequence", is by register time and column time, both on the display (Figure 2-5) and on the delay line (Figure 2-6). Note that all R times in C2 occur before the R times in C3, the R times in C3 before the R times in C4, etc.

To move data from R1 to R2, the data must be stored (delayed) until R2 time occurs. To move data from R2 to R1, the data must be moved ahead in time (advanced) because R1 occurs before R2. To move data from a register in C2 time to the same register in C3 time, the data must be delayed (stored) until that C3 time occurs. The delay or advance in time is determined by the type of shift.

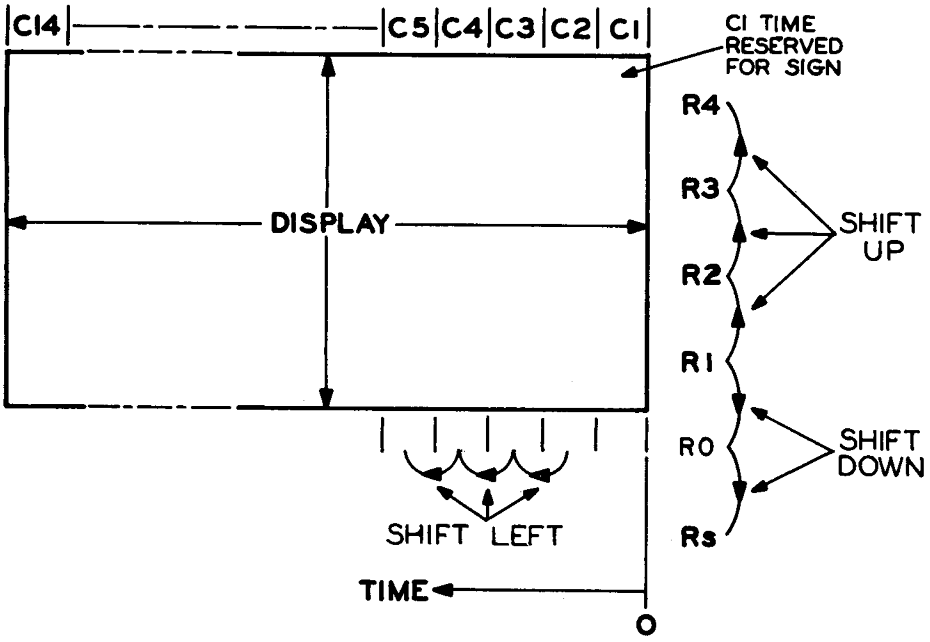


Figure 2-5. Display Shifting

b. SHIFT UP. To shift up means that on the display (See Figure 2-5) the registers will move up: R1 data to R2, R2 data to R3, R3 data to R4, and R4 data will be lost. However, in terms of data sequence, each register data is delayed one register time and the data placed in the next succeeding register (See Figure 2-6).

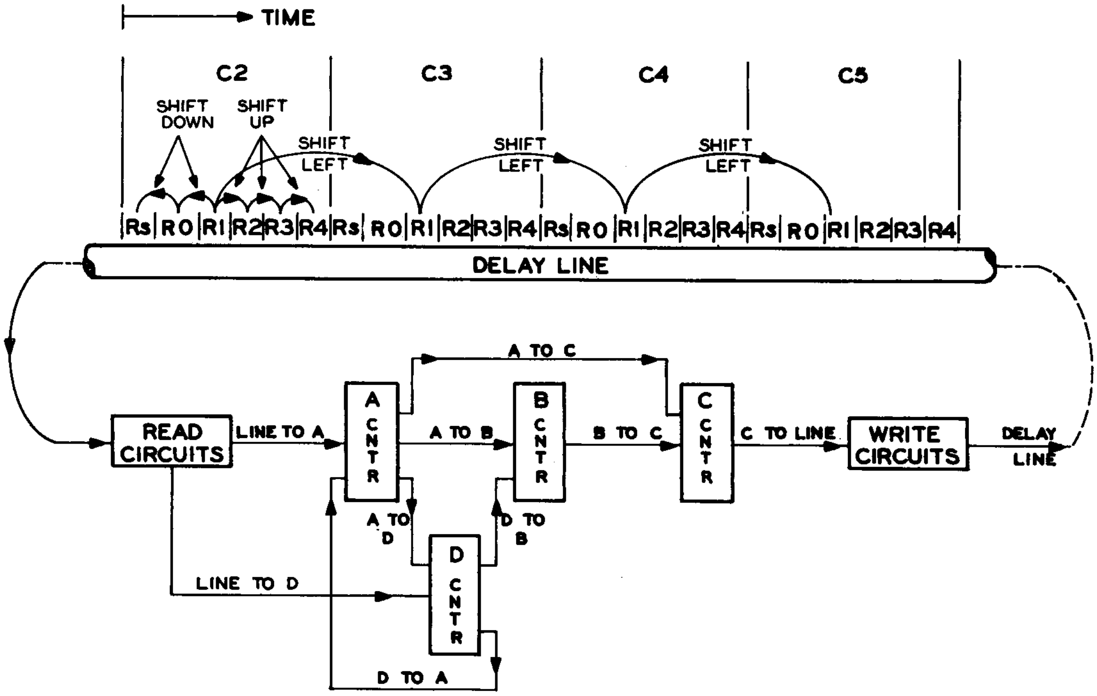


Figure 2-6. Data Shifting

Shift up is done by shifting A to D, holding the data in D for one register time, then shifting D to B, which places each register data in turn into the next succeeding R time. Since R1 time is displayed ahead of R2 time, if R1 data is placed in R2 time, it will appear as shifted up on the display. However, placing R1 data in R2 time places it later (delayed) in the data sequence on the delay line.

c. SHIFT LEFT. Shift left is very similar to shift up and uses the same sequence of shifts, but at different times and for a longer delay. Shift left, limited to R1 and R2 by the function control circuits, is done by shifting the selected register A to D, holding for one C time, and shifting D to B at the corresponding R time in the next C time. Since R1C2 time is displayed ahead of R1C3 time, if R1C2 data is placed in R1C3 time, it will appear as shifted left on the display. However, placing R1C2 data in R1C3 time places it later (delayed) in the data sequence on the delay line.

d. SHIFT DOWN. To shift down means that on the display the registers will move down; R4 data to R3, R3 data to R2, R2 data to R1. However, in terms of data sequence, each register data will be advanced one register time and the data is placed in the next preceding register.

Shift down is accomplished by shifting A to C, instead of A to B. Since one R time in B counter has been bypassed, data effectively moves ahead in the data sequence, and will be written on the delay line sooner. Since R1 time is displayed ahead of R2 time, if R2 data is placed in R1 time, it will be shifted down on the display. However, placing R2 data in R1 time places it earlier (advanced) in the data sequence on the delay line. (Note that in Shift Up and Shift Down two undisplayed registers will be affected; R0 and RS.)

6. DELAY LINE CIRCUITS

The delay line is a storage device. Together with the counters, the delay line keeps numbers in the machine as long as the machine is idling. The delay line also provides storage for data during the steps and operations necessary for the completion of a function.

The delay line circuit (Figure 2-7) is electromechanical. That is, a portion of the circuit is mechanical in nature, and the rest of the circuit is electrical. The two portions work together to produce a finite time delay for the extremely fast, (by comparison) electronic data operations. This delay in time effectively stores the data for the time of delay, approximately five (5) milliseconds (.005 seconds).

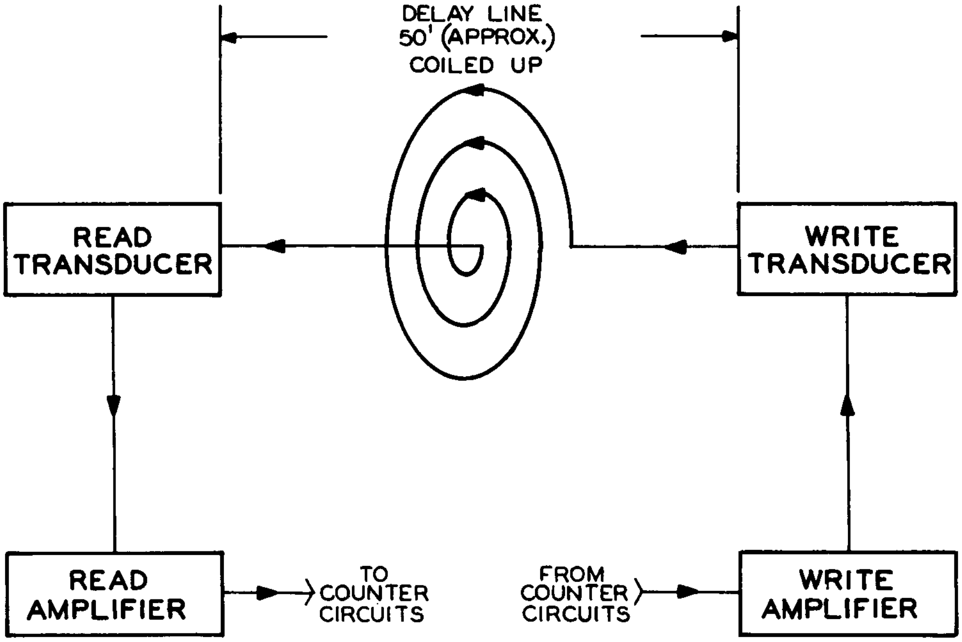


Figure 2-7. Delay Line Functional Diagram

a. DELAY LINE. The delay line is made of nickel alloy wire about the diameter of a mechanical pencil lead. A physical twist (torsion) of one end of the wire takes a definite amount of time to reach and affect the other end. The amount of time is primarily determined by the length of the wire, which is approximately fifty (50) feet. To save space, the delay line is coiled up and mounted in such a manner that movement of the mechanical waves along the wire are not affected.

b. TRANSDUCERS. The transducers are the components that change electrical pulses into mechanical movements (twists) of the delay line, and, conversely, change mechanical twists into electrical pulses.

A transducer is mounted at and connected to each end of the delay line. They are designated as: Launch or Write transducer and Receive or Read transducer.

(1) Write Transducer. The action of the Write transducer is dependent on the fact that the element nickel changes physical length when subjected to a change of magnetic field. This is called "magnetostriction".

The Write transducer consists of two nickel ribbons mounted in the centers of two coils of wire. A pulse of current (data pulse) from the write amplifier causes a proportional change in the magnetic field of the coils. This magnetic field change causes the nickel ribbons to change dimension lengthwise. One ribbon shrinks, the other ribbon expands. This gives a push-pull effect on the wire of the delay line, and thus gives more twist for each pulse than if one ribbon were used. The effective result of each pulse of current is to produce a momentary twist in the delay line that will travel to the other end at a finite speed.

(2) Read Transducer. The Read transducer is basically the same as the Write transducer. However, while the function of the Write transducer is to convert electrical pulses to mechanical twists of the delay line, the function of the Read transducer is to convert delay line twists to electrical pulses.

The delay line twists at the Read transducer momentarily distort the shape of the nickel ribbons. One ribbon will be stretched, the other compressed, and together they give a push-pull action that gives more effect on the coils for each delay line twist than if one ribbon were used. The change of shape of the nickel ribbons induces a voltage in the coils surrounding the ribbon. This voltage is the output of the Read transducer.

c. AMPLIFIERS. The delay line circuitry contains two amplifiers; a Write amplifier and a Read amplifier.

(1) Write Amplifier. The purpose of the Write amplifier is to convert (data) pulses of voltage to current pulses of a value adequate to actuate the Write transducer.

(2) Read Amplifier. The purpose of the Read amplifier is to build up voltage pulses from the Read transducer (that represent data on the delay line) to a value adequate to actuate the counter circuits.

7. IDLE

Idling is the progression of data from the delay line, through the counters, and back onto the delay line, with no change in data sequence. The machine is said to be "idling" when no function is being performed. Data progression through the counters in idle is: Line to A, A to B, B to C, C to line. Since the data sequence is preserved, there is no change in time relationships between the data.

8. FUNCTION CONTROL

A function is a series of internal machine operations that produce a specified result. An internal machine operation consists of one or more steps that occur at times that are specified by the function control circuits. The time relationships are established by signals from the timing circuits.

The functions of the EC-130 are initiated from the keyboard by the function keys. There are two classes of functions: Operational functions and Arithmetical functions. Operational functions can be designated as those functions that arrange the data for the arithmetical functions that will take place. The operational functions are: Digit Entry, Store, Recall, Repeat, Clear Entry and Clear All. The arithmetical functions are: Add, Subtract, Multiply, and Divide.

9. DISPLAY

Display occurs only during idle. Periodically during idle, the data in display registers R1 through R4 is copied in the D counter. The display circuits then convert the D counter data into a visual equivalent for display. The data sequence for display is: R1 data for all C times, R2 data for all C times, R3 data for all C times, and R4 data for all C times.

For example; assume R1C2 data from the delay line has been counted into the A counter. When an A to B shift occurs during idle, an A to D shift also occurs, which copies the R1 data into D counter. While the rest of the C2 data progresses through the counters, and until R1C3 data has been counted into the A counter, the R1C2 data in the D counter is being converted and displayed. Then, when R1C3 data is shifted A to B, an A to D shift occurs which copies the R1C3 data into the D counter. Again, while the rest of the C3 data is progressing through the counters, R1C3 data in the D counter is being converted and displayed. This progression continues until the R1 data in all display C times has been converted and displayed. Then R2 data will be displayed in the same manner, followed by R3, and finally R4.

10. DISPLAY CIRCUITS

Numbers which exist in the machine in electronic form must be converted to their visual equivalent correctly placed on the display. The display circuitry converts the numbers to a visual equivalent and provides for proper placement on the CRT.

a. CATHODE RAY TUBE (CRT). The CRT in the display circuitry is the device that converts electron energy into a visual equivalent. The CRT is composed of three functional sections: the electron gun, the deflection plates, and the phosphor coating (screen) on the inside of the face of the tube.

(1) Electron Gun. The electron gun in the CRT is the source of electrons that, when they strike the screen, generate visible light. The gun consists of a cathode, which is the source of electrons; a grid, which controls the number of electrons; and anodes that focus the electrons into a thin, pencil-like beam.

There are three controls associated with the functioning of the electron gun. They are: Intensity, Focus, and Astigmatism. The Intensity control, which is connected to the grid, establishes the brightness of the trace on the CRT. The Focus control, which is connected to the anodes, establishes that the beam is at its smallest diameter at the CRT screen. The Astigmatism control, which is also connected at the anodes, establishes the "roundness" of the electron beam. Adjustment of these controls is covered in section 3 of this manual.

(2) Deflection Plates. The deflection plates control the instantaneous position of the electron beam (spot) on the face of the CRT. Control is exercised by the voltage relationship between the plates of each set of plates. The Horizontal plates control the horizontal position, and the Vertical plates control the vertical position. Together, their action can place the spot caused by the electron beam at any position on the screen.

(3) CRT Screen. The coating on the inside of the face of the CRT is called a "Phosphor". The phosphor has the property of changing the energy of the electron beam into visible light. The amount of light (brightness) is determined by the average number of electrons in the beam, and that, in turn, is controlled by the Intensity control.

The phosphor has a further quality called "persistence". Persistence is the continued emission of light for a period of time after the beam has moved. This quality permits the "writing" and viewing of a complete display that looks as if it were drawn instantly even though it is developed by the rapid movement of a single spot.

b. HIGH VOLTAGE SUPPLY. In order that visible light be produced by the phosphor when struck by electrons, the electrons must have a certain energy level, or speed. They are accelerated to this speed by a high potential (2400 volts) between the cathode, the accelerating anodes, and the face of the tube. The high voltage supply develops this voltage.

c. CHARACTER FORMATION. All of the characters displayed are derived from a basic figure eight composed of several portions called "Segments" (See Figure 2-8). Each segment is identified by a number that refers to the technical manner of segment generation. The number is used only for identification of the segment. Not all of the segments are used. Of those that are used, the Blanking circuits control which segments will be displayed and thus which character appears on the display. For example; 0 is the basic figure eight with segments 7 and 14 kept blanked. Character 2 is the basic figure 8 with segments 0, 3, and 14 kept blanked.

For a more pleasing and readable display, certain characters are modified. Figure 1 is offset to the right; figure 7 is slightly offset to the left; segment 7, when used as a part of figure 3, is slightly shortened; Decimal Point is segment 13 modified to appear as a dot; and Minus Sign is Segment 14 drawn in place of segment 7, with all other segments blanked.

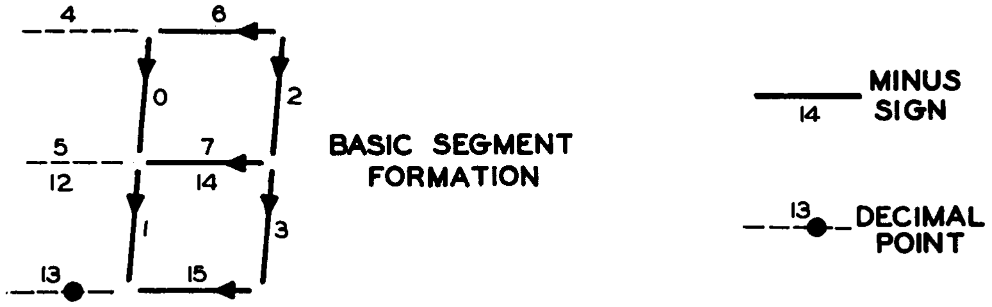


Figure 2-8. Basic Character Formation

d. DISPLAY DEFLECTION. The deflection circuits develop the voltages that are applied to the deflection plates to move the spot caused by the electron beam, which forms the characters on the screen in their proper position. The horizontal deflection voltage is slightly modified by the slant amplifier to give the displayed characters a more pleasing appearance.

e. BLANKING CIRCUITS. Each segment for each character space on the CRT is developed for all possible character spaces every time a display is called for by the internal machine timing. However, some segments are never drawn on the CRT, and for different characters certain segments are not used. The Blanking circuits determine which segments will be displayed, thus what character will be "written" on the CRT. The time relationships between the blanking circuits and the deflection circuits determine "what" character will appear "where" on the CRT. The timing relationships are specified and controlled by the basic machine timing circuits.

The blanking circuits also keep the entire CRT blanked while a function is being performed, since any display that appeared while data shifted or changed would be meaningless.

B. BASIC CIRCUITS

In the EC-130 there are certain types of circuits that are used very often and in many circuit configurations. These circuits will be discussed only to the extent of their primary characteristics. The applications of these circuits will be discussed in the circuit configuration in which they are used.

1. FLIP-FLOP (FF)

The Flip-flop (FF) is a type of circuit that is used in the Counters, Entry Phase Counter (EPC), Decimal Point Counter (DPC), and as the primary initiation of many circuit functions. Therefore, it is very important to understand the basic action of a typical FF. This is covered in Lesson 20 of Friden Electronic Course.

The basic circuit configuration of a bi-stable FF is as illustrated in Figure 2-9(A). Note the symbol for a FF also shown in Figure 2-9(C). The first thing to be noticed in the FF schematic (A) is the symmetry. Each transistor has the same number of inputs, resistors, capacitors, etc. and is connected to the other transistor and the power sources in the same manner.

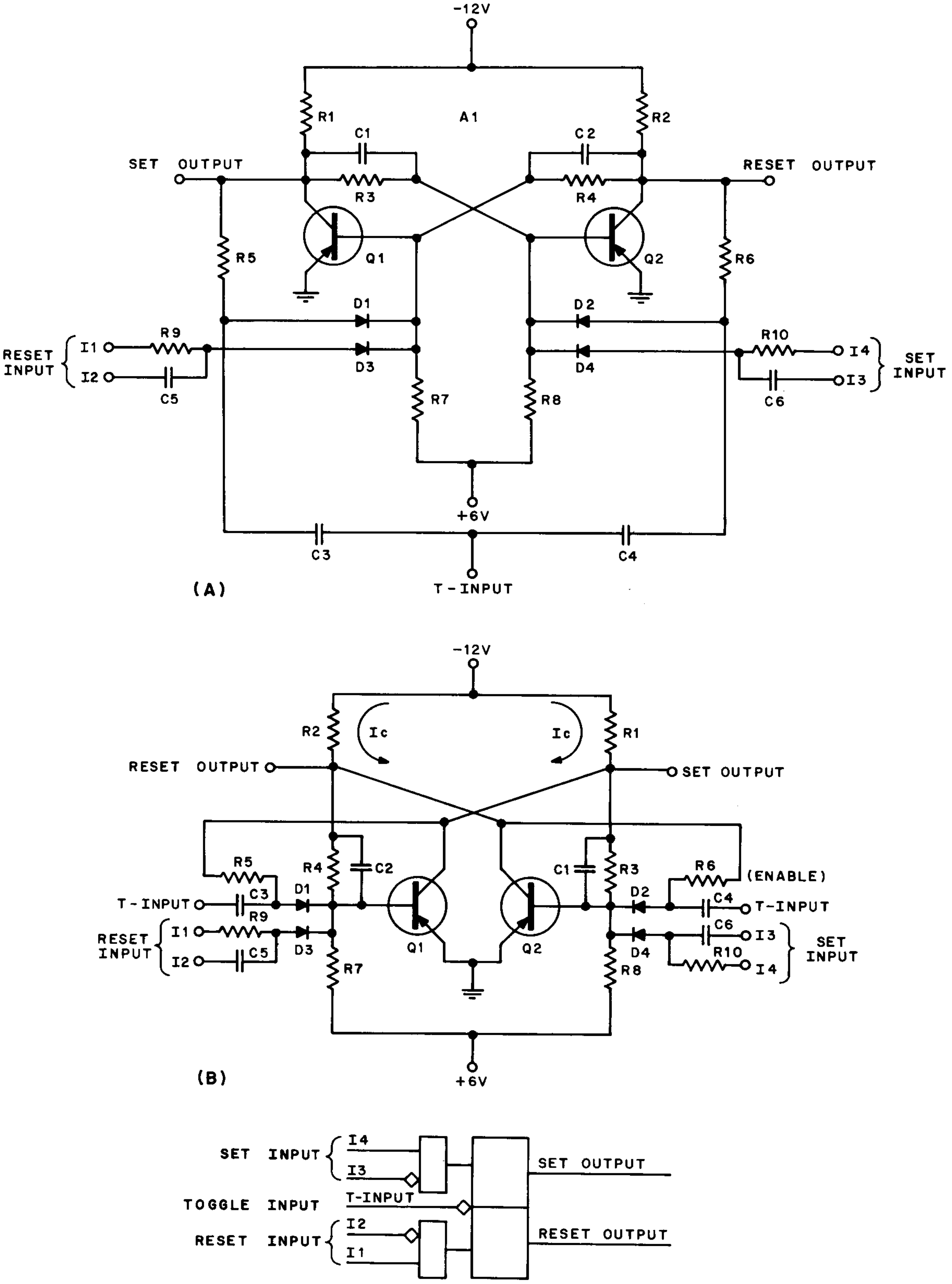
In the circuit redrawn as Figure 2-9(B), assume Q1 conducting and Q2 cutoff. The voltage dividers in each base circuit are as illustrated in (B).

The collector current of Q1 through R1 makes Q2 base positive and Q2 is cutoff. Since Q2 is cutoff, there is no Q2 collector current through R2, and Q1 base is negative. This condition will remain until an external signal is applied. As shown, external signals can be applied to the base of each transistor. T-input and gate inputs are False to True transitions, called positive transitions. It can be seen that applying a positive transition to the base of a transistor already cutoff by a positive voltage could do no more than cut the transistor further off. However, a positive transition applied to the base of a transistor turned on by a negative voltage would tend to lower conduction by some amount. Assume a positive transition at C3. This will pass through the isolating diode (D1) and be applied at the base of Q1. This would lower conduction of Q1, collector current of Q1 through R1 would decrease, and, since this collector current is the determining factor in the positive voltage on Q2 base, Q2 base would go less positive and eventually Q2 starts to conduct. Q2 collector current through R2 increases the IR drop across R2 and the voltage changes in a direction that makes Q1 base more positive. Q1 collector current decreases still more through R1, Q2 base goes still more negative, Q2 collector current increases through R2, and Q1 base goes still further positive. The regenerative process, once started by a positive transition at C3, continues until Q1 is cutoff and Q2 saturated and occurs very quickly. This condition remains until a positive external signal at C4 reverses the Q1-Q2 conditions. This is called a bi-stable FF since the circuit has two stable conditions, and can be "Flipped" from one, and "Flopped" back to the other. Hence, the name Flip-flop.

C1 and C2 are commonly called "speed-up" capacitors. Immediately that the junction of R2 and R4 goes more positive because of increased Q2 collector current, this change is applied to the base through C2 to cause the effect on Q1 to occur faster. C1 provides a fast path for the change at the junction of R1 and R3 caused by the lowered collector current of Q1 to be felt at the base of Q2. Thus, the circuit change is faster than it would be without the capacitors.

As can be seen by the circuit schematic, the T-input is connected to both transistor bases, but since a positive transition is applied, the transition can only affect the transistor that is on. Thus a signal at T-input changes the state of the FF from set to reset, or vice-versa, depending on the condition when the T-input signal is applied.

In some specific applications it is desired to specifically set or reset a FF. This is the reason for the AC gates at the base of each FF. The action of AC gates is covered under Basic Logic discussion. The output of an AC gate will be a positive transition. Note that the reset signal is applied to the set side of the FF, and the set signal is applied to the reset side of the FF. This is because a positive transition can only affect the transistor that is on. Thus, when the Flip-flop is set, Q1 is on, Q2 is off. In reset, Q2 is on, Q1 is off. Therefore to put the FF in a set condition, Q2 must be turned off by a positive transition, thus the "set" signal is applied to the reset transistor base. Further note, if the transistor is already set, Q1 is on and Q2 off and applying a positive set signal to the base of Q2 can have no effect since Q2 is already off. Thus, applying a set signal to a FF already set has no effect. The opposite is also true, in that applying a reset signal to a FF already reset can have no effect.



D130-117W

Figure 2-9. Basic Flip-Flop Circuit

Outputs from the FF are taken from the collector. Q1 is arbitrarily designated set, and Q2 designated reset. If the FF is set, Q1 is conducting and the output is True, approximately 0 volts, because Q1 is in saturation and all of the -12 is dropped across R1. If the FF is reset, however, Q2 is conducting, Q1 is cutoff and the set output will be low, approximately -12 volts, because there is no collector current through R1, thus no IR drop. Of course, since R1 is a part of a voltage divider between -12 and +6, there will still be some current through R1, and set output will be somewhat less than -12; however, the set output will be a definitely negative value, designated logic 0, or False, which will distinguish it from a logic 1, or True, that is approximately 0 volts.

To distinguish between set and reset outputs of a given FF, for instance A1, the set output is given the designation A1 and the reset output given the designation A2. It is important to remember, however, that A1 can be either True or False depending on whether the FF is set or reset, and the same is true of A2.

2. INVERTER

An inverter is a circuit configuration that inverts the polarity of signal applied to its base. Thus when a positive signal (True) is applied to an inverter the output goes negative (False).

The basic configuration of an inverter is as shown below.

Note the divider in the base circuit. The resistor values are chosen so that, with the input diode disconnected, the junction of R2 and R3, which is the base connection, is some negative value that puts Q1 in saturation. With the transistor saturated, collector current drops all the -12 volts across R4, and the output is 0 volts (True).

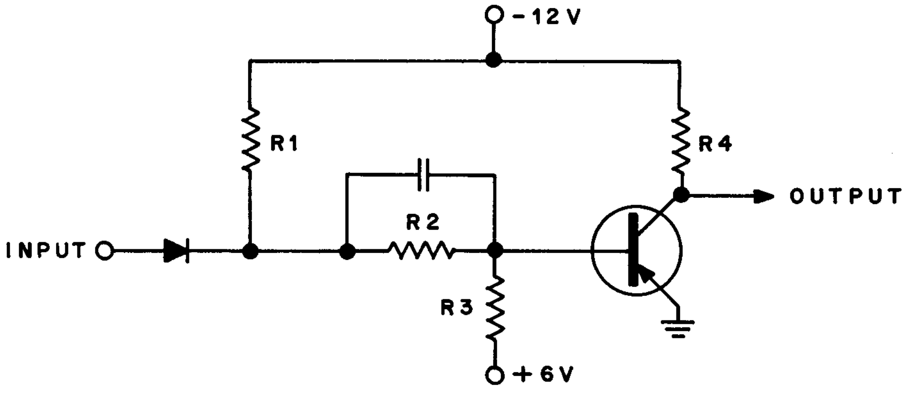
Now assume the anode of the diode goes True (0 volts). The cathode of the diode is returned to -12 volts, and the diode conducts. Diode current drops all the -12 volts across R1, and the junction of R1 and R2 goes to 0 volts. At this time, there is no -12 volts applied to the entire voltage divider and the junction of R2 and R3 goes positive since all that is being divided by R2 and R3 is +6 volts. This positive voltage at the base cuts the transistor off. With Q1 cut off, there is no collector current through R4, and the output goes to -12 volts (False). Thus the application of a True (0 volt) signal to the input of the inverter circuit causes the output to go False (-12), and the input is inverted.

Now assume the anode of the input diode goes False (-12 volts). The diode stops conducting because the junction of R1 and R2 is more positive than -12. Since -12 volts is now applied to the entire voltage divider, the junction of R2 and R3 will be some negative value that saturates Q1. With Q1 saturated, collector current through R4 drops all the -12 volts, and the output goes to 0 volts (True). Thus, again, the input condition is inverted. Note the capacitor across R2. It is called a "speed-up" capacitor and the purpose is to turn the inverter on (or off) faster, as in the FF.

One of the many uses of inverters in the EC-130 is at the output of logic gates. If the gate output is True, it is inverted False, and vice-versa. The specific uses of the inverters will be covered in the circuit configuration discussion, as applicable.

3. EMITTER-FOLLOWER

The emitter-follower circuit configuration is widely used in the EC-130 when a signal from a source such as an inverter is used in many places simultaneously, thus constituting a heavy load on the inverter. No discussion of the emitter-follower will be given since it is adequately covered in Lesson 18 of the Friden Electronic Course.



C. COUNTER CIRCUITS

In the EC-130, the designation "counters" refers to the group of circuits that, in addition to counting, perform shift (transfer) functions. There are four groups of FF's termed counters, designated A, B, C, and D. Each counter circuit consists of five FF's interconnected with each other and with the other counters in a manner that enables the counter circuits to perform the functions of counting or shifting as the logic control circuits designate.

The two functions of the counters, counting and shifting, will be discussed separately on a block diagram basis for ease of understanding because the interconnections are complex.

1. COUNTING

There are two types of counters in the EC-130, Up Counters and Down Counters. The action of each is very similar and the counter FF's are interconnected in very much the same manner.

a. UP COUNTER. The FF's designated A1, A2, A3, A4, and A5 are connected as an Up Counter. (See Figure 2-10.) Counting up means that, starting from the specific initial condition of all FF's reset, addition of pulses one by one, called "advance" (or increment), will change the FF settings in an orderly progression that will represent the number of pulses (See Truth Table for Up Counter).

As illustrated, the FF's are drawn in a ring for easier comprehension of the interconnections. In fact, this type of circuit is sometimes called a "Ring Counter". Note that the set and reset outputs from one FF are directly connected to gates at the set and reset inputs for the next FF, with the exception that A5 set is connected to A1 reset gate, and A5 reset connected to A1 set gate. The crossover, or reversal, of this set of FF connections enables five FF's to attain settings representing a total count of ten (10), 0 through 9.

The gates at the inputs to the FF's are called AND gates, and will be referred to as AC gates. (See Basic Logic discussion.) They consist of a resistor-capacitor combination in which the polarity of voltage applied to the resistor acts as enable on the gate, and the + transition voltage (Increment) applied to the capacitor acts as the actual set or reset signal. In other words, the set side signal from A2 applied to the AC gate at the set input of A3 will enable A3 to set if, and only if, A2 has already set, meaning that A2 set output is True. Note that A2 set will only enable A3 to set. It takes a + transition signal at the capacitor side of the AC gate input of A3 to actually set A3. The transition signal, which in this case is "Increment", is applied to all FF's simultaneously but only those FF's that are enabled by the previous FF in the chain will actually change state.

For example, five (5) increment pulses into the counter will place all FF's in a set condition. A5 set output will be True and is applied as a permit to the AC gate at the reset input of A1. The next pulse in (6th pulse) will reset A1, which represents a count of six (See Truth Table). The reset of A1 will permit the next pulse in (7th pulse) to reset A2, which is defined as count of 7. Thus, the crossover of set-reset connections between A5 and A1 enables progression from a setting representing five to a final setting of 0, which brings all FF's back to reset condition and the next pulse in starts counting up from 0 through 9, or a total of 10.

It is important to remember that the connections between the set-reset of each FF only enable the FF's to change settings. The actual change of setting occurs when a + transition is applied to the capacitors of the AC gates. If this pulse is not applied, the FF's will not change state regardless of the enable conditions at the FF AC gates.

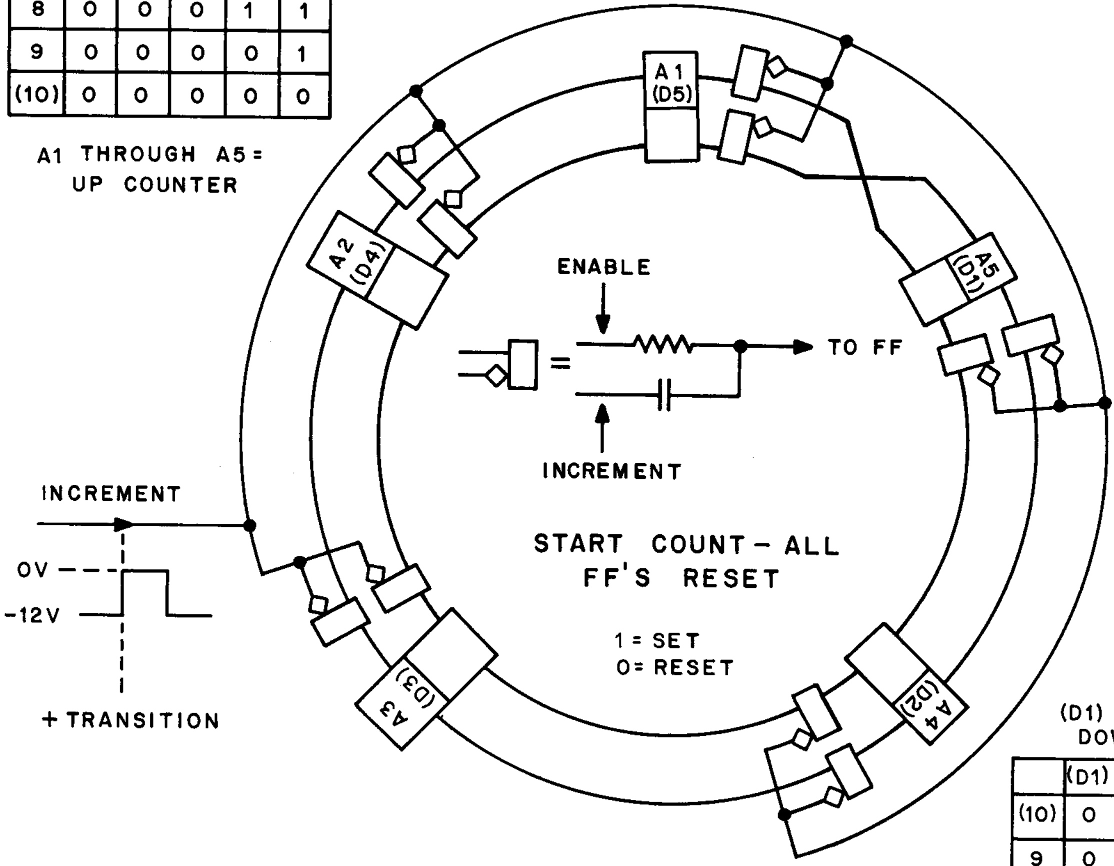
b. DOWN COUNTER. The FF's designated (D1), (D2), (D3), (D4), and (D5) are connected as a Down Counter. (See Figure 2-10.) Counting down means that, starting from the specific initial condition of all FF's reset, addition of pulses one by one, called "Increment", will change the FF's in an orderly progression that will represent the number of pulses (See Truth Table for Down Counter), but in a downward direction.

As in an Up Counter, there is a correspondence between the set and reset outputs of one FF to the set and reset AC gates of the next FF in the chain, with one exception. The exception is that D1 set is connected to D5 reset gate, and D1 reset connected to D5 set gate. The crossover, or reversal, of this set of leads indicates that D5 will be the first FF to set because only D5 has an enable applied to the AC set gate at the initial condition of all FF's reset. Therefore, the first pulse sets D5, and all others remain reset. Reference to the Truth Table for a Down Counter indicates that this is the condition for representing number nine (9). The second Increment pulse sets D4 FF, therefore the new setting of the five FF's will represent the number eight (8). With the condition that 0 (all FF's reset) represents 10, then the addition of pulses one by one will count down the pulses until a total of ten (10) pulses places all FF's in a reset condition (See Truth Table) and starts the count down over again.

	A1	A2	A3	A4	A5
0	0	0	0	0	0
1	1	0	0	0	0
2	1	1	0	0	0
3	1	1	1	0	0
4	1	1	1	0	0
5	1	1	1	1	1
6	0	1	1	1	1
7	0	0	1	1	1
8	0	0	0	1	1
9	0	0	0	0	1
(10)	0	0	0	0	0

TRUTH TABLE
UP COUNTER

A1 THROUGH A5 =
UP COUNTER



(D1) THROUGH (D5)
DOWN COUNTER

	(D1)	(D2)	(D3)	(D4)	(D5)
(10)	0	0	0	0	0
9	0	0	0	0	1
8	0	0	0	1	1
7	0	0	1	1	1
6	0	1	1	1	1
5	1	1	1	1	1
4	1	1	1	1	0
3	1	1	1	0	0
2	1	1	0	0	0
1	1	0	0	0	0
0	0	0	0	0	0

TRUTH TABLE
DOWN COUNTER

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Figure 2-10. Basic Counter Functional Diagram

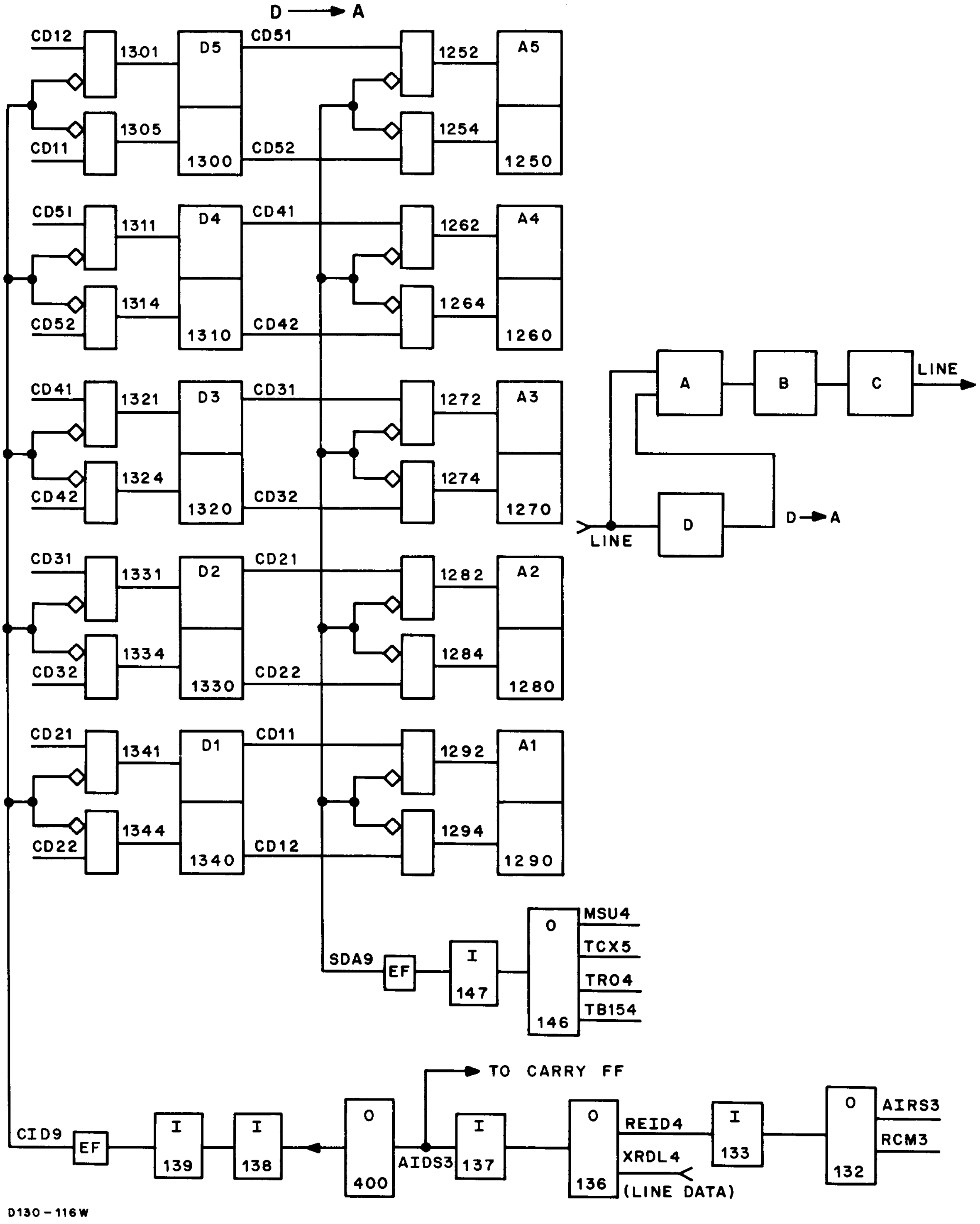


Figure 2-11. Digit Complement, Functional Diagram

It is interesting to note that the actual settings of A1 through A5 and D1 through D5 represent the same number in both an Up Counter and a Down Counter. However, the number of pulses into the counter necessary to arrive at that number is different, and determined by whether it is an Up Counter or a Down Counter. Thus, two Increment pulses into an Up Counter results in a setting representing two (2), while two Increment pulses into a Down Counter results in a setting representing eight (8).

In the EC-130, certain arithmetic functions require taking the complement of a digit. If two pulses (representing digit 2) are counted into an Up Counter, the counter setting will represent 2 (A1, A2, set; A3, A4, A5 reset). The same two pulses into a Down Counter will set the counter to represent 8 (D5, D4 set; D2, D3, D1 reset). Since the 10's complement of a one digit number is the difference between that number and ten, counting into a Down Counter set to 0 gives the 10's complement of a digit, while counting into an Up Counter set to 0 gives a setting representing that digit. In some cases, the Down Counter starts from a condition of 9, which will give the 9's complement of the number counted in.

c. DIGIT COMPLEMENT. Logic action in the EC-130 requires the taking of the complement of a digit in some functions. This is accomplished by CID9 (Increment D), which counts data off the line into D Counter. Since D Counter is a "Down" Counter, the final setting of D becomes the complement of the digit represented by the data pulses. After the data is counted in D, D Counter setting is shifted D to A (SDA9) or D to B (SDB9), which inserts the data in the proper place in the data sequence as specified by the control logic.

Increment D (CID9) (Figure 2-11) is controlled by O-132. If either input is True, the output of O-132 is True. The development of "Increment D in Subtract" (AIRS3) and "Complement" (RCM3) inputs to O-132 will be discussed when applicable to a specific machine function. True output of O-132, inverted False by I-133, designated REID4, is applied to enable O-136 acting as a -AND. XRDL4 input consists of negative data pulses from the Read Amplifier and represents data from the delay line. As long as O-136 is enabled, the output will go False with each negative XRDL4 pulse. False pulses from O-136 are inverted True by I-137, designated AIDS3. The first True pulse from I-137 (AIDS3) is used to set Carry FF, which signifies in the logic that a complement of the digit is taken. Once Carry is set, any further AIDS3 True pulses from I-137 have no further effect.

AIDS3 True pulses from I-137 are also applied through O-400 to I-138, and inverted False. False pulses from I-138 are inverted True by I-139, designated CID9, and applied to D Counter. D Counter will count down by 1 for each CID9 pulse. Therefore, the final setting of D will represent the complement of the number of data pulses.

Shift D to A (SDA9) is developed by I-147 controlled by O-146 acting as a -AND. The logic of the development of the signals into O-146 will be discussed when applicable to specific machine function.

D Counter data derived during a complementing action can also be shifted D to B when specified by machine logic. D to B shift is exactly as described in Shift Up and Shift Left except for the specific time of the shift, which is controlled by machine logic through O-130. The development of the logic controlling this shift will be covered when applicable to a specific machine function.

2. DATA SHIFTING.

Shifting is the moving of data settings between counters. In this application the counters are not necessarily correctly named because no counting is involved. However, the same counters used for counting are also used for shifting when machine logic so indicates.

a. SHIFT UP. A Shift Up operation requires that data be delayed 48 usec in time. Hence, an extra 48 usec period of data time is introduced by shifting A to D, then D to B. Since the display of the data sequence is fixed and starts with the earliest data in time, then reinserting the data at a later data time places the data in a different position when displayed. Since the data is delayed one register time (48 μsec) then the data moves up one register on the display. This is designated as Shift Up because of the apparent movement of the data even though the action is really data delay.

Shift A to D (SAD9) is developed by I-124 (Figure 2-12) controlled by O-123 acting as a -AND. When machine logic specifies A to D shift, SEAD4 at O-123 will be False and enable the gate. Now, when TB154 goes False at the end of each R time, the output of O-123 goes False and, inverted True by I-124, will be the + transition (SAD9) that shifts A Counter setting to D Counter.

D Counter has been reset to 0 before this data shift occurs. However, even if D were not zero, the data shift would still occur and D Counter would end up with the same settings as A Counter, and whatever data was in D Counter would be effectively replaced, thereby discarded.

As the A Counter data setting is shifted to D Counter, A Counter is reset to zero and used for the next data in the data sequence. Once D Counter has changed setting, when a + shift transition signal, designated SDB9, is supplied to B Counter then the D Counter setting will move to B Counter.

Shift D to B (SDB9) is developed by I-131 controlled by O-130 acting as a -AND. When machine logic specifies a D to B shift, SEDB4 at O-130 will be False and enable the gate. Now, when TB154 goes False at the end of each R time, the output of O-130 goes False and, inverted True by I-131, will be the + transition (SDB9) that shifts D Counter setting to B Counter.

The exact times of the A to D and D to B shifts in Shift Up are determined by the EC-130 control logic and will be discussed when applicable to specific machine function.

b. SHIFT LEFT. Shift left moves the digits one column left on the display, hence the name Shift Left. The sequence of shifts, A to D and D to B, is the same. Except for the time data is held in the D Counter before being shifted D to B, the counter action in Shift Up and Shift Left is the same. The time difference between Registers is 48 μsec, thus delaying the data for 48 μsec moves the data one register up on the display and one register later in the data sequence. The time difference between a register in one column and the same register in the next column is 288 μsec. Thus, if a given register is shifted A to D, then shifted D to B 288 μsec later, the data is placed in the same register time but displayed one column to the left and placed one column later in the data sequence.

The exact times of the A to D and D to B shifts in Shift Left are determined by control logic and will be discussed when applicable to specific machine function.

c. SHIFT DOWN. Control logic of the EC-130 can call for an advance of data in the data sequence, which will appear on the display as a Shift Down, hence the name given this particular shift.

Normal progression of Data is: Count in A, Shift A to B, Shift B to C, Count C to line. In each of these shifts and counts, the data is in one counter for a period of one register time (48 μsec) but, since the data relationship is not changed, the relative position of the data on the display does not change. However, if the data were to bypass the time usually spent in B Counter (48 μsec), the data would be placed on the Delay Line one register time earlier (advanced) in the data sequence and appear on the display as having been moved down by one register.

Shift Down executes a shift that bypasses B Counter, which effectively advances data in the data sequence and, on the display, the registers appear to shift down.

The counter interconnections applicable to Shift A to C are illustrated in Figure 2-13. Set and reset outputs of A Counter are connected to AC gates at the corresponding set and reset inputs of C Counter. When the + transition signal, SAC9, is applied to all C Counter AC gates simultaneously, C Counter assumes the same setting as A Counter, thus A data setting is shifted A to C. By other means, A Counter is reset to 0 and becomes ready for new data to be counted or shifted in.

Shift A to C (SAC9) is developed by I-120 controlled by O-119 acting as a -AND. O-119 is enabled by I-118 output, designated SEAC4. The input to I-118 is machine logic that specifies A to C shift. TC153 inhibits O-119 during C15 time so that no A to C shifts occur during C15 time. At any time other than C15 time, TC153 is False and enables O-119. When machine logic specifies A to C shift, SEAC4 is False. When TB154 goes False at the end of each R time, all inputs to O-119 are False and the output is False. False output of O-119, inverted True by I-120 provides the + transition (SAC9) that shifts A Counter setting to C Counter.

In the machine logic control, whenever an A to C Shift is called for, the B to C Shift is inhibited. This is done so that data does not enter C Counter from two places simultaneously. However, this could easily leave data in B Counter so that, when normal shift progression again occurred, this data could move into the data sequence improperly. An additional shift, D to B, is called for whenever A to C is initiated. Since D Counter is set to 0 by other means, this places B Counter to zero with the first D to B shift. From then on, the D to B shift keeps placing zeroes in the B Counter until no more A to C shifts are called for by the control logic. For explanation of the D to B shift and logic refer to Shift Up.

d. IDLE. As illustrated in Figure 2-14, counter A set and reset outputs are connected directly to AC gates at the set and reset inputs of Counter B, and Counter B set and reset outputs are connected directly to AC gates at the set and reset inputs of Counter C.

The sequence of shifts called A to B and B to C is a part of machine operation called "idle". When in this operation, no arithmetic is being performed, no change of data sequence is occurring, and display is taking place. During idle, the data in the machine leaves the delay line via the Read Amplifier, counts into A Counter, Shifts A to B

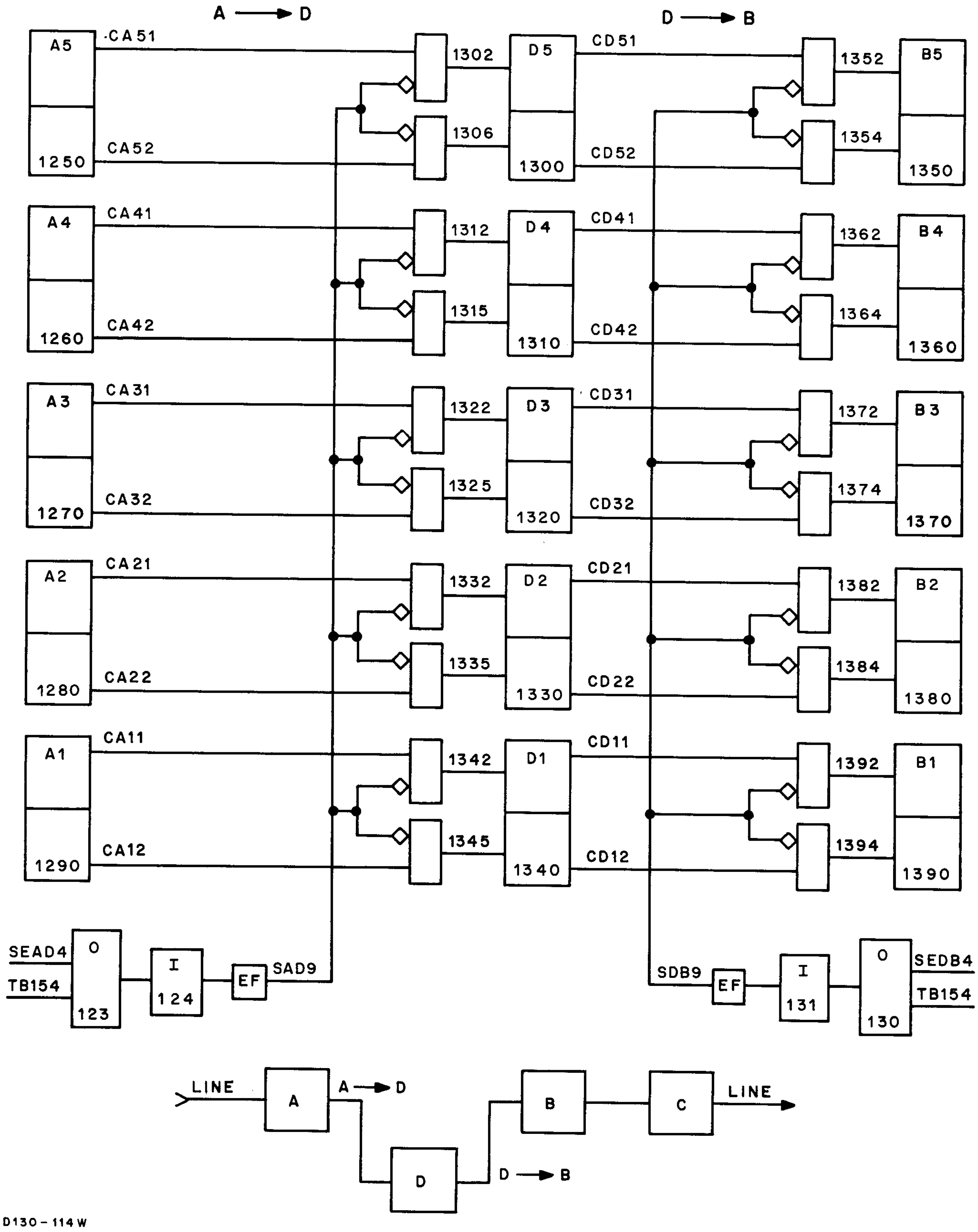
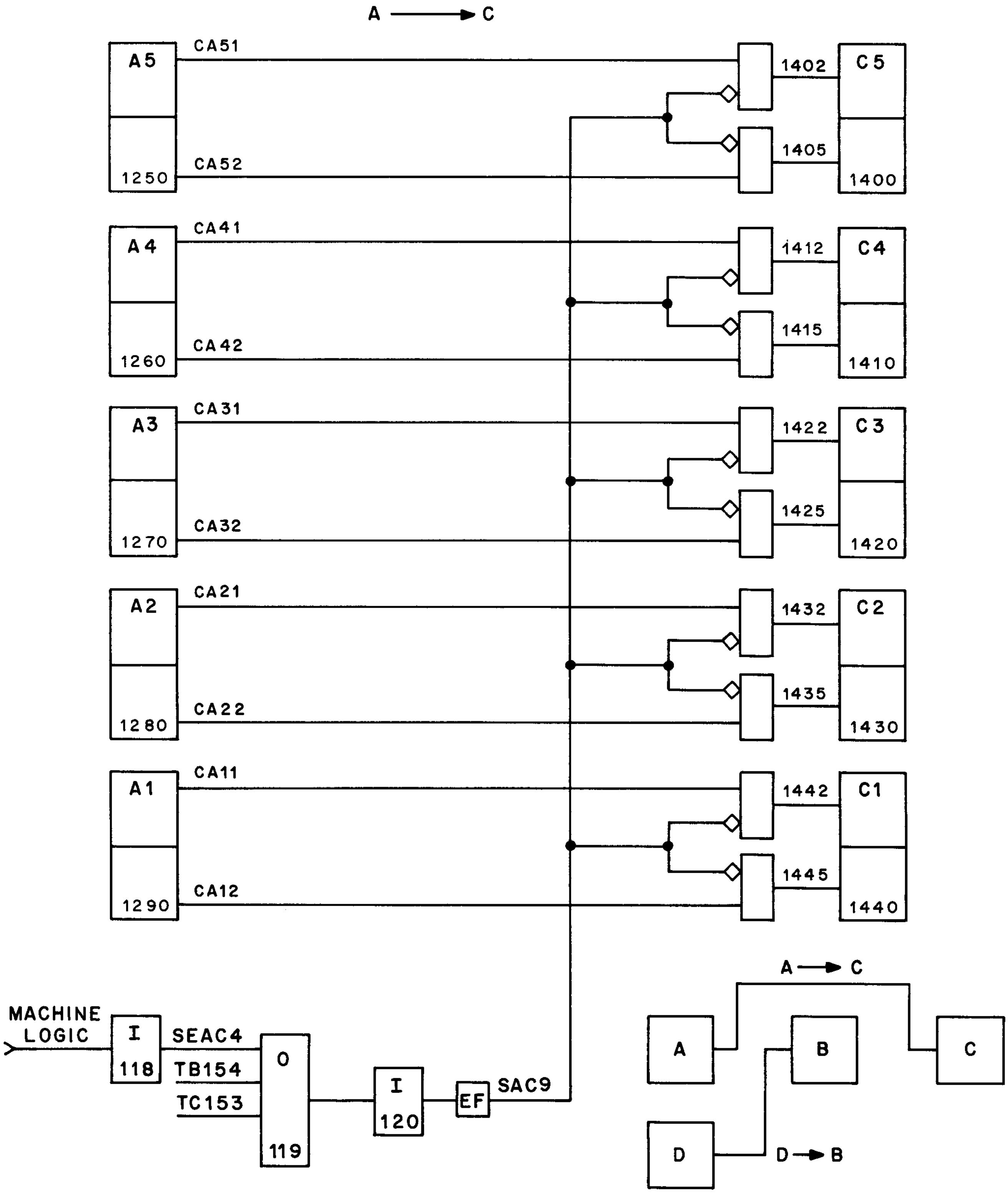


Figure 2-12. Shift Up or Left, Functional Diagram



D130-113W

Figure 2-13. Shift Down, Functional Diagram

and B to C, and is counted from C Counter back into the delay line via the Write Amplifier. After entering the delay line, data is delayed about 5 milliseconds then counted into the A Counter again and follows the same progression as before. The data is said to be "circulating in the machine".

It is often difficult to comprehend the fact that A sets B (Shift A to B) at the same time B sets C (Shift B to C). This can occur because AC gates have a "memory" of their last state which persists until the capacitor of the gate can reach a new voltage level through the resistance. This action is described under Basic Logic discussion and in Lesson 20 of Friden Electronic Course. Thus, even though B Counter sets immediately to the state of A Counter, C Counter AC gates retain a "memory" of the last state of B Counter for a short time. The shift B to C transition initiates the change of C Counter to the previous B Counter state through this "memory" characteristic of C Counter FF AC gates. This "memory" is characteristic of all AC gates and is utilized when shifting data between counters, as well as in other circuits.

The transition at the B Counter FF AC gates that specifies the shift of A Counter setting to B Counter (SAB9) is developed by I-127 controlled by O-126 acting as a -AND. The enable signal on O-126 is the output of I-125, designated SEAB4.

There are two inputs to I-125. One is from the machine logic through I-129 (SEDB4), and the other is C0 time (TC03) through an isolation diode.

Remembering that the Sync pulse is in C0R3B3 time, if Shift A to B (and B to C) were not enabled for C0 time, then the Sync pulse would not be shifted through the counters and back on the delay line. O-126 is enabled for C0 time by TC03 (True) applied through the isolation diode to I-125 and inverted False. At the end of C0R3 time. TB154 goes False because the Sync pulse has started the timing chain, and the output of O-126 goes False. False output of O-126 inverted True by I-127 is applied through an emitter-follower as SAB9 to B Counter FF AC gates. Since only those FF gates that are enabled by the condition of A Counter FF's are affected by SAB9 False to True transition, then only those B Counter FF's are affected and B Counter assumes the same setting as A Counter.

At times other than C0, TC03 is False and the isolation diode is back-biased, thus has no effect at the input of I-125. During C1 through C15 time the output of I-129 (SEDB4) inverted False by I-125, designated SEAB4, provides the enable to O-126. During Idle, SEDB4 will be True, inverted to False by I-125, and provide an enable to O-126. This means there will be an A to B data shift every B15 time during idle. The action of I-129 during machine logic will be discussed where applicable.

At the same time that A Counter setting shifts to B, B Counter setting shifts to C, and in the same manner except that the transition signal is SBC9. SBC9 is developed by I-117 controlled by O-116 acting as a -AND. The enable signal on O-116 is the output of I-115, designated SEBC4, and O-116 will be enabled when SEBC4 is False.

There are two inputs to I-115. One is from the machine logic, and the other is C0 time (TC03) through an isolation diode. The action of TC03, which enables Sync pulse to be shifted during C0 time, is exactly as described under Shift A to B. Also, the action of machine logic through I-115 is the same as in I-129 in the Shift A to B discussion.

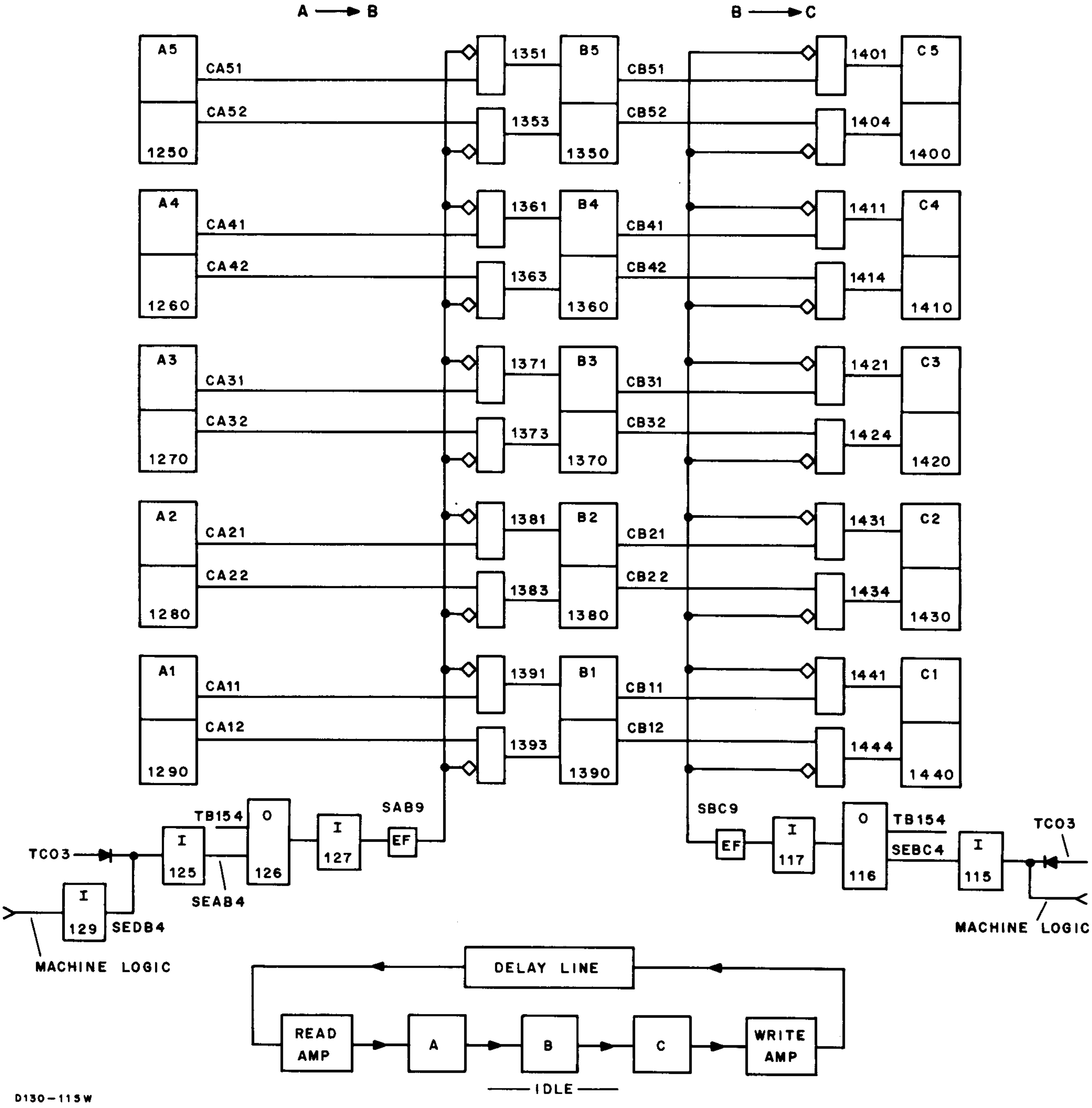


Figure 2-14. Idle Condition, Functional Diagram

D. DELAY LINE CIRCUITS

The delay line is a storage device. Together with the counters, the delay line keeps numbers in the machine as long as the machine is idling. The delay line also provides storage for data during the steps and operations necessary for the completion of a function.

The delay line circuit is electromechanical. That is, a portion of the circuit is mechanical in nature, and the rest of the circuit is electrical. The two portions work together to produce a finite time delay for the extremely fast (by comparison) electronic data operations. This delay in time effectively stores the data for the time of delay, approximately five (5) milliseconds (.005 seconds).

1. DELAY LINE

The delay line is made of nickel-iron alloy wire about the diameter of a mechanical pencil lead. A physical twist (torsion) of one end of the wire takes a finite amount of time to reach and affect the other end. The amount of time is primarily determined by the length of the wire, which is approximately fifty (50) feet. To save space, the delay line is coiled up and mounted in such a manner that movement of the mechanical waves along the wire are not affected. (See Figure 2-15.)

2. TRANSDUCERS

The transducers are the components that change electrical pulses into mechanical movements (twists) of the delay line, and, conversely, change mechanical twists into electrical pulses. (See Figure 2-16.) A transducer is mounted at and connected to each end of the delay line. They are designated as Write transducer and Read transducer.

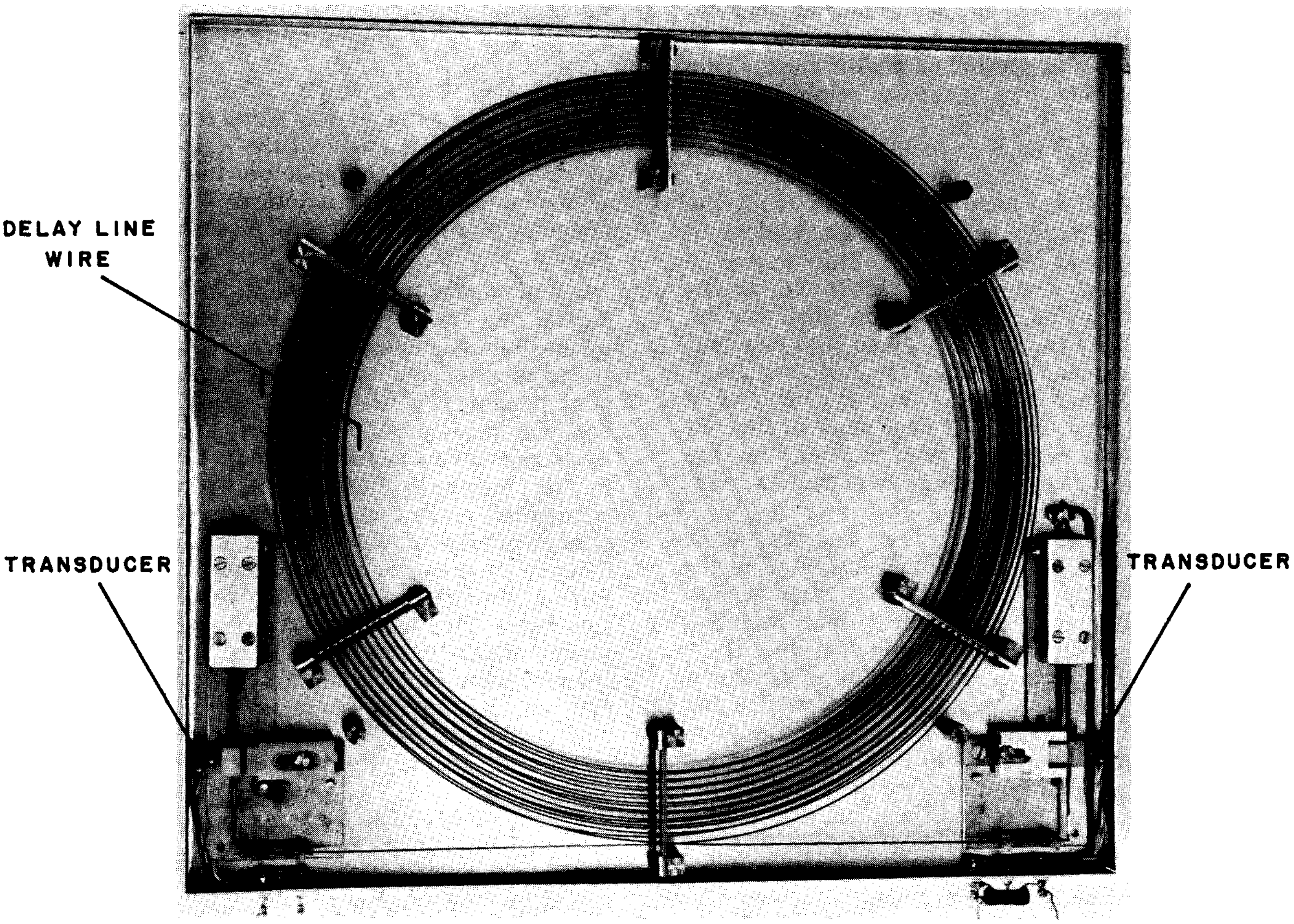


Figure 2-15. Delay Line, Physical Arrangement

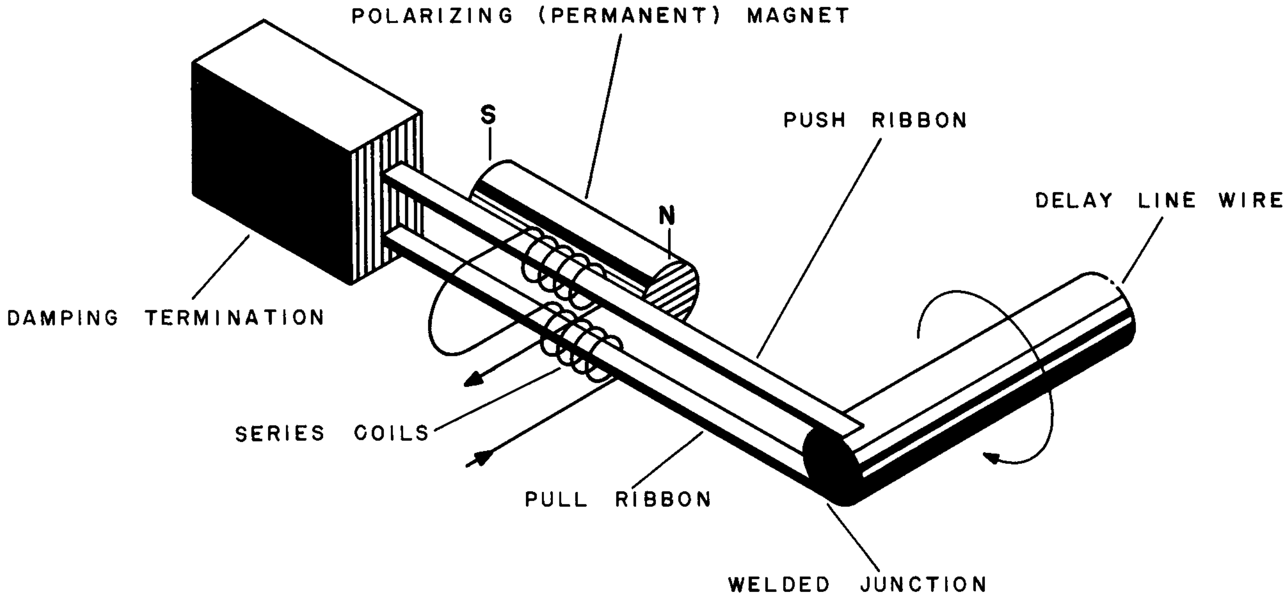


Figure 2-16. Transducer Functional Diagram

a. WRITE TRANSDUCER. The action of the Write transducer is dependent on the fact that the element nickel changes physical length (shrinks) when subjected to a change of magnetic field. This phenomenon is called "magnetostriction".

The Write transducer consists of two nickel ribbons mounted in the centers of two coils of wire. A pulse of current (data pulse) from the write amplifier causes a proportional change in the magnetic field of the coils. This magnetic field change causes the nickel ribbons to change dimension lengthwise. One ribbon shrinks, the other ribbon expands. This gives a push-pull effect on the wire of the delay line, and thus gives more twist for each pulse than if one ribbon were used. The effective result of each pulse of current is to produce a momentary twist in the delay line that will travel to the other end at a definite speed.

The purpose of the permanent magnet in the write transducer is to provide a means of push-pull effect by the nickel ribbons. Since nickel shrinks further when a magnetic field becomes stronger, the "polarizing" magnet sets up a fixed shrinkage of the ribbons. In one coil of the Write transducer the field induced by the "Write" pulse of current will aid the fixed field and that ribbon shrinks further, thus a pull to the lower end of the delay line wire. The same current pulse in the other coil opposes the fixed field and that ribbon expands toward its normal (without any fixed field) length, thus a push on the upper end of the wire. Therefore, the current pulse through the coils has twice as much effect on the ribbons and a larger "twist" than if only one coil and ribbon were used.

The damping termination is to prevent undesired mechanical reflections to be set up on the nickel ribbons.

b. READ TRANSDUCER. The Read transducer is basically the same as the Write transducer. However, while the function of the Write transducer is to convert electrical pulses to mechanical twists of the delay line, the function of the Read transducer is to convert delay line twists to electrical pulses.

As the delay line wire twists at the Read transducer, one ribbon is expanded and the other compressed. A fixed field from the permanent magnet is surrounding the coils and the effect of the ribbon changes is to increase the flux density in one coil and decrease the flux density in the other coil. A change in flux density is equivalent to a change in the magnetic field and a voltage is induced across the coils that is directly proportional to the change in flux density. Since the change in flux density is directly proportional to the change in ribbon dimension, which is caused by the delay line twist, then the induced voltage of the coils is proportional to the delay line twist. In the Read transducer the placement of the coils is such as to give the maximum output per twist of delay line. The output of the coils in the Read transducer is connected directly to the Read Amplifier.

3. READ AMPLIFIER

The purpose of the Read Amplifier is to amplify the output of the Read transducer to a level that is adequate to actuate the counter circuits to which they are applied, and to shape the pulse for optimum action in the counter circuits.

In the Read Amplifier Schematic, as illustrated in Figure 2-17, the 1.5K and 100 pf across the transducer coils are to damp out transients. The output of the Read coils is applied to the base of Q1. Q1 is biased class A and the amplified Read pulse is coupled to the base of Q2, which is also biased Class A, where it is further amplified. The collector load of Q2 contains a 2K potentiometer, which provides a means of gain control, designated "Shaper Gain". The output of Q2 is taken from the arm of the potentiometer and capacitor coupled to Q3 base for further amplification by Q3. The output of Q3 is from the collector load resistor, at which point there is a test point for waveform examination. From Q3 the amplified Read pulse is applied to Q4 and Q5 which comprise a wave-shaping circuit.

Q4 is an emitter-follower coupled to inverter Q5 through a capacitor. Under conditions of no read pulse, Q5 is biased on and Q4 emitter side of the coupling capacitor is about -5.6 volts. Under signal conditions, the positive excursion of the Read pulse through Q3 is about 5 volts, as illustrated. However, as soon as the fixed bias is overcome at the base of Q5, at a change of about 1.5 volts in a positive direction through the coupling capacitor, the Read pulse turns Q5 off and the collector of Q5 goes to -12 volts.

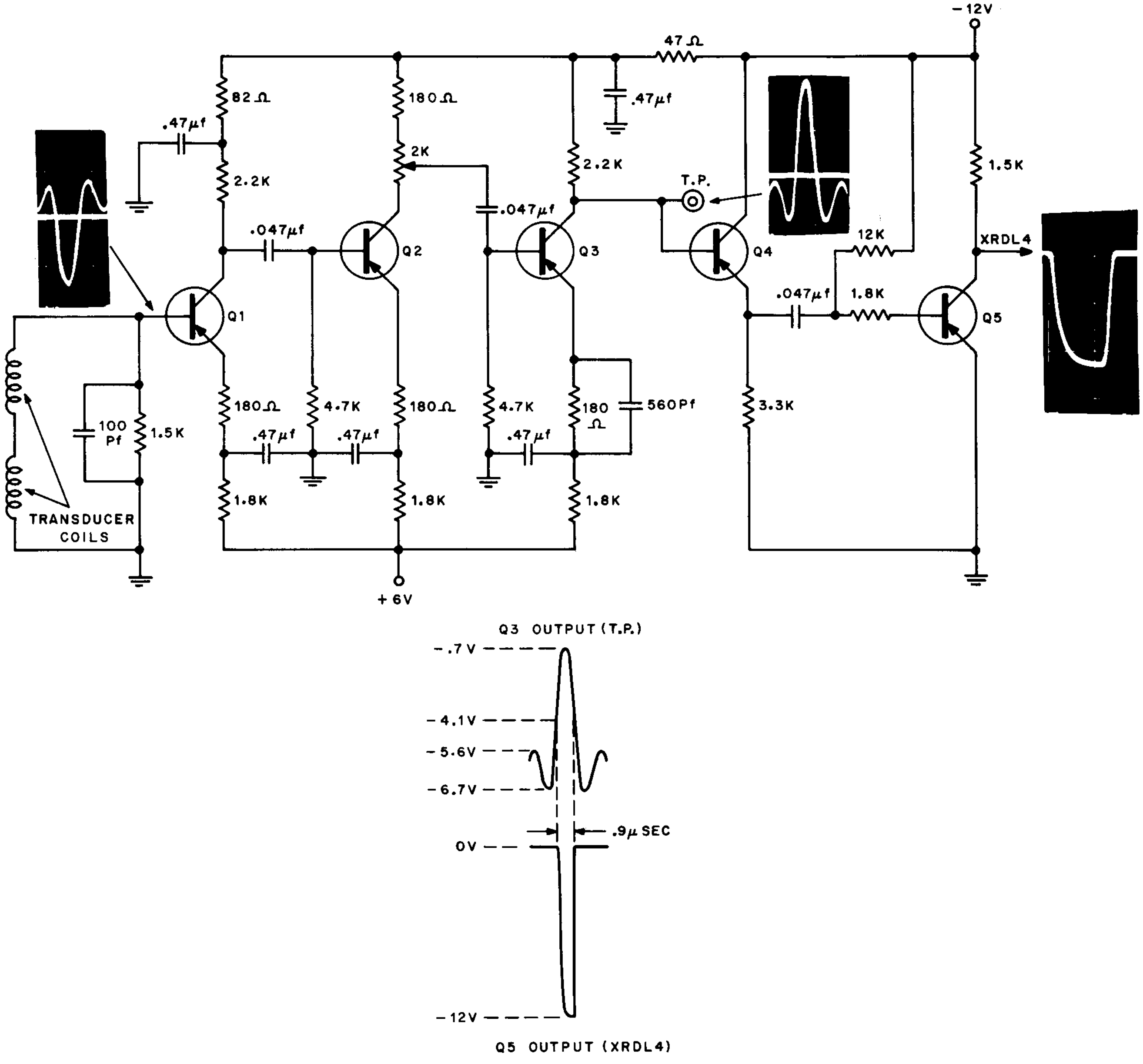


Figure 2-17. Read Amplifier, Schematic Diagram

Q5 remains cut-off until the Read pulse at Q4 emitter again reaches about -4.1 volts, when Q5 turns on and Q5 collector goes to effective ground. The negative excursion of the Read pulse can have no effect on Q5, since Q5 is already heavily on. The net result of the Read pulse through Q4 on Q5 is to turn off Q5 for the period of time that the pulse is above -4.1 volts, and to turn Q5 on again when the pulse again reaches -4.1 volts. The output pulse at the collector of Q5 is a steep-sided square wave pulse about .9 µsec wide which varies from 0 volts to -12 volts and is of an optimum shape and amplitude to actuate the counter circuits. The logic term name of the Read pulse is designated XRDL4.

4. WRITE LOGIC

Before the circuitry of the Write amplifier is discussed, the Write logic development must be understood.

The Write logic (Figure 2-18) has three design purposes. One is to provide a means of converting data information in C Counter into an equivalent number of torsional twists of the delay line to represent this data. Another is to provide a means of placing a "Sync" pulse on the line that will act to synchronize the timing chain with the data on the line (See Basic Timing discussion). Finally, the Write logic provides a means of erasing all data on the line by inhibiting write action.

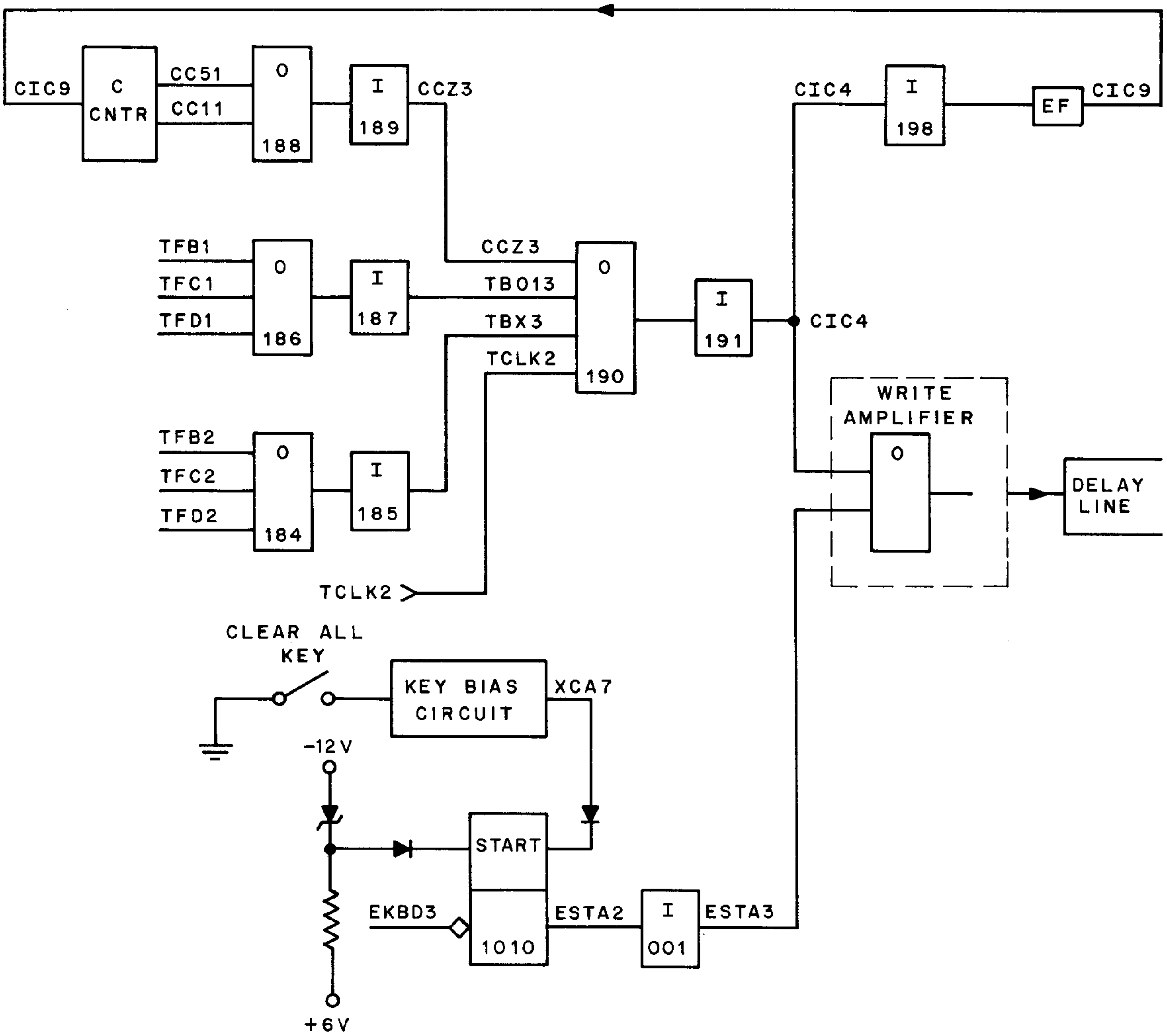


Figure 2-18. Write Amplifier, Logic Diagram

a. SYNC PULSE. When the EC-130 is first turned on, the zener-voltage-divider sets Start FF. Now, when any function at the keyboard initiates EKBD3, start FF resets. The False to True transition at Start reset output (ESTA2), inverted True to False by I-001, designated ESTA3, is applied to an OR gate in the Write Amplifier. The OR gate is enabled at this time because of CCZ3 being True at O-190 and inverted False by I-191, designated CIC4. As will be explained in Write Amplifier discussion, this OR gate acts as a -AND and the Write Amplifier places a Sync pulse on the delay line when Start FF resets. After this one transition, Start FF remains reset, ESTA3 remains False, and the OR gate in the Write Amplifier remains enabled by ESTA3, and the CIC4 True to False transition becomes the initiator of data pulses that put torsional twists on the delay line.

b. INCREMENT C (CIC4). CIC4 is developed by I-191 controlled by O-190. If all inputs to O-190 are False, and then one goes True, the output of O-190 makes a False to True transition, which is inverted True to False by I-191, designated CIC4.

Three inputs to O-190 are inhibiting inputs at specific times to prevent writing on the line. I-185 controlled by O-184 inhibits O-190 during B14 and B15 time, designated TBX3. I-187 controlled by O-186 inhibits O-190 during B0 and B1 time, designated TB013. I-189 controlled by O-188 inhibits O-190 if C Counter is zero, meaning there is no data in C Counter. If there is data in C Counter, either C1 or C5 will be set. If either CC11 or CC51 at O-188 is True, the output is True and, inverted False by I-189, designated CCZ3, acts to enable O-190. The net result of these three inputs on O-190 is to enable O-190 from B2 through B13 time as long as there is data in C Counter (CCZ3 False).

The other input to O-190 is TCLK2 from the timing chain. TCLK2 will transition False to True every 3 μsec when the timing chain is running (See Basic Timing discussion). When TCLK2 transitions at O-190, the output of O-190 transitions False to True, and is inverted True to False by I-191, designated CIC4.

CIC4 is applied to the Write Amplifier OR gate and also to I-198. The True to False output transitions of I-191 caused by TCLK2 at O-190 are inverted False to True by I-198, and applied through an emitter-follower as CIC9 to C Counter. Each CIC9 pulse counts C Counter down by one until C Counter reaches zero (C Counter is a "down counter"). When C Counter reaches zero, meaning no data left in C, CC11 and CC51 inputs to O-188 are both False and, inverted True by I-189, bar any further TCLK2 transitions at the output of O-190. As long as TCLK2 transitions are enabled at O-190 output by all other inputs being False, CIC4 will not only count C Counter down but also act at the OR gate of the Write Amplifier.

c. CLEAR ALL. To clear all data from the machine means to erase all data from the delay line. This is accomplished by inhibiting the Write Amplifier OR gate.

A Sync pulse was placed on the line and the Write Amplifier OR gate was enabled by the output of I-001 (ESTA3) controlled by the Start FF. If Start FF is set, reset output (ESTA2) is False and inverted True by I-001, designated ESTA3, is applied to inhibit the OR gate at Write Amplifier input. If the OR gate is inhibited, then no data is placed on the line and the machine is cleared of data in one word time.

Set of Start FF is initiated by pressing CLEAR ALL Key on the keyboard which, through a voltage divider network, designated Key Bias circuit, initiates a positive transition (XCA7) at set side of Start FF output, and sets Start FF.

5. WRITE AMPLIFIER

The purpose of the write amplifier is to shape the input pulses, which are about 1.5 μsec wide, into current pulses about 1 μsec wide and amplify the current pulses to a level adequate to actuate the Write transducer, which places the torsional twists on the Delay Line wire.

The write amplifier (See Figure 2-19) not only places the Sync Pulse on the line when ESTA3 goes True to False but also provides a data pulse every time CIC4 goes True to False. (See Write Logic discussion.)

The OR gate at the input of Q1 in the Write Amplifier acts as a -AND. ESTA3 (from I-001) enables this gate when Start FF is reset by EKBD3. CIC4, which goes True to False because of TCLK2, provides a False (-12) output at the base voltage divider of Q1. When CIC4 at the input of the OR gate is True, Q1 is biased off. With Q1 off -12 volts is at the Q1 collector side of the 470 pf coupling capacitor to Q2. The base voltage divider biases Q2 on, and the Q2 side of the 470 pf capacitor is about .7 volts negative. At this time C1 is charged to about 11 volts.

Now, when CIC4 input goes False at the OR gate, the base voltage divider of Q1 has -12 volts applied and Q1 base goes negative, which turns Q1 heavily on. With Q1 on, Q1 collector goes effectively to ground and C1 sees a transition from -12 to ground, and must discharge. The 11 volt positive transition is coupled through C1 to the base of Q2 and Q2 turns off.

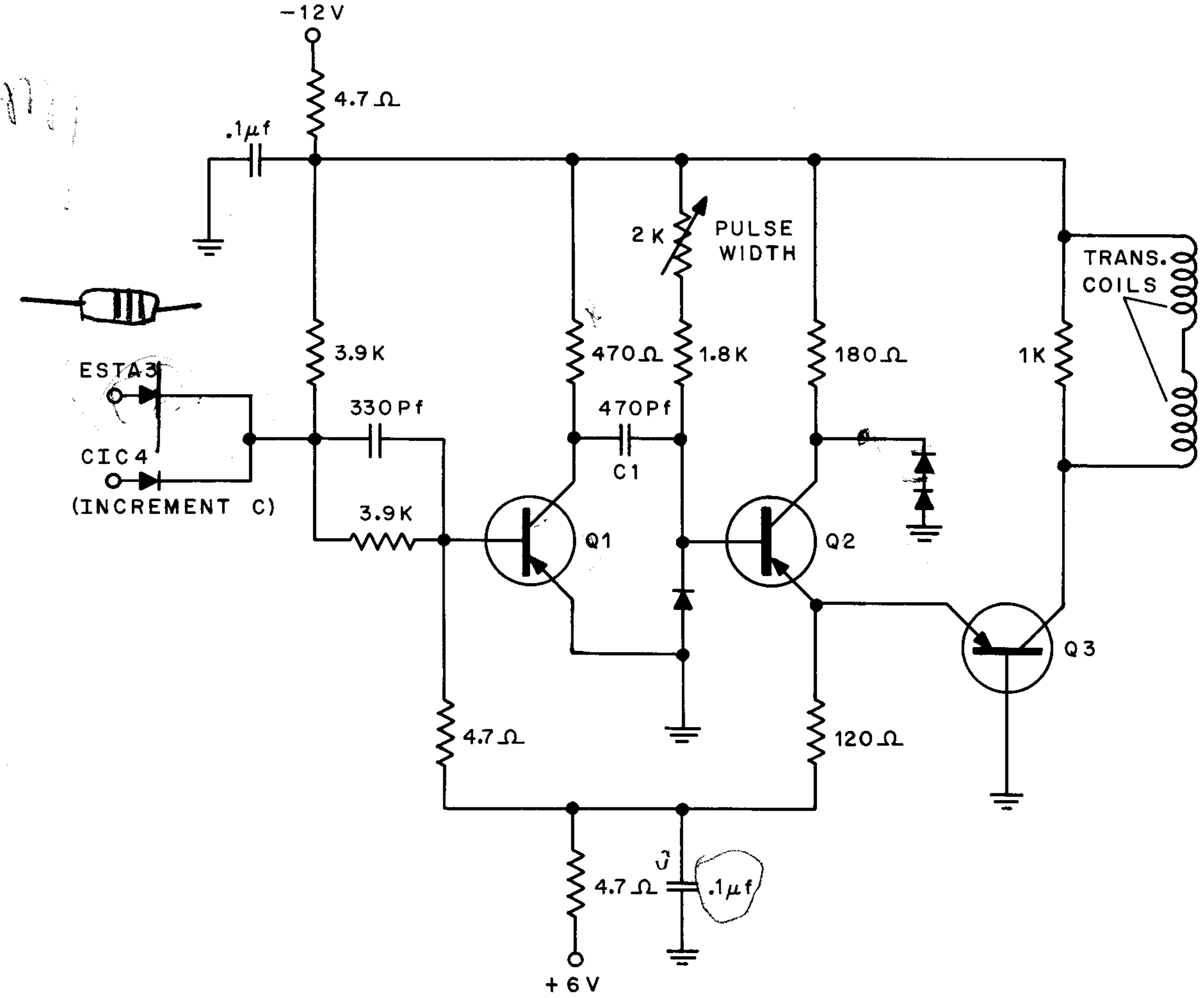


Figure 2-19. Write Amplifier, Schematic Diagram

C1 must change by 11 volts through a 1.8K fixed resistance and a 2K variable potentiometer. By adjustment of the 2K potentiometer the length of time Q2 remains off can be adjusted to slightly less than 1 μsec, (.96), which is the optimum pulse width. The length of time Q2 is off is dependent only on the RC time of change of C1, thus, while CIC4 at the input of Q1 is 1.5μsec wide, it has no effect on the pulse width at the emitter of Q2, which is dependent only on the length of time between Q2 off and Q2 on.

The emitter of Q2 is connected to the emitter of Q3, which is connected in a grounded-base configuration. When Q2 is on, the emitter of Q3 is slightly negative, and Q3 is biased off. When Q2 is off, the emitter of Q3 goes toward +6 volts and Q3 turns heavily on. When Q3 turns on, Q3 base to emitter voltage drop, which is about .2 volt, clamps Q2 emitter to about +.2 volt. With Q3 on, a current path is established between -12 volts, the write transducer coils, Q3, and +6 volts and a large current will flow. When a current pulse flows in the Write transducer coils, a twist is produced in the delay line wire.

The diode in the base circuit of Q2 is a part of the base voltage-divider and limits Q2 base to about -.5V. The series diodes in Q2 collector circuit form a voltage-divider with the 180 ohm resistor and ensure that Q2 collector never exceeds about -1V. This limits the voltage across Q2 to a value that protects Q2 from excessive power dissipation.

There will be one torsional twist of the delay line for each CIC4 pulse into the write amplifier and at the same time C Counter will count down by one. Since O-190 will be enabled until C Counter goes to zero (CCZ3 True), each TCLK2 pulse will put a pulse (twist) into the delay line and count C Counter down by one.

Assume a C Counter setting of 2. Two TCLK2 transitions will place twists onto the delay line and simultaneously count C Counter to zero. When C Counter reaches zero, O-190 is inhibited and no more TCLK2 pulses are permitted to the Write Amplifier via I-191. Thus a one to one correlation will exist between the number of pulses necessary to count C Counter to zero and the number of TCLK2 pulses permitted into the Write Amplifier. Therefore, C Counter data setting is translated into an equivalent number of twists on the delay line.

In approximately 5 ms these delay line twists arrive at the other end of the delay line and are converted back to electronic pulses by the Read Amplifier to actuate A or D Counters in a manner that counts into these counters an equivalent of the number of pulses on the delay line for a given R time (See Counters discussion).

E. BASIC LOGIC

Applied logic can be described as the progression of a series of controlled actions that lead to a specific result. The logic control in the EC-130 is by means of logic gates. The gates most used are called OR, AND, and AC. The absence of a polarity reference means, by definition, a positive gate. That is, if ANY input to an OR gate is positive, the output is positive. In the case of an AND gate, ALL inputs must be positive for the output to be positive. An AC gate is a special form of an AND gate.

Logic design in the EC-130 specifies that a True output be 0 volts (approximately) and that a False output be some voltage more negative than 0 volts, for explanation assumed to be -12 volts. True (0 volts) in the EC-130 can also be referred to as Logic 1. False (-12 volts) in the EC-130 can be referred to as Logic 0. The terms are synonomous and interchangeable, although True and False will be used throughout this manual.

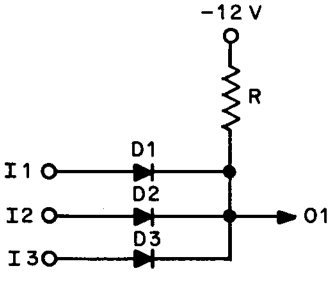
1. OR GATE

A diode positive OR gate, usually designated as simply O, is constructed as shown.

Diodes conduct when the cathode is more negative than the anode, or, to say it oppositely, when the anode is more positive than the cathode. When a diode conducts it is essentially a short circuit, disregarding the small IR drop across the diode, and whatever voltage is at its anode will appear at the cathode in this configuration.

Assume I1, I2, and I3, are False (-12V). No diode is conducting, no current flow through R, and O1 is -12 volts, which can be specified as False, or Logic 0. Now assume I1 to be True (0V). D1 conducts heavily, current flow through R drops all the -12 volts and O1 goes to 0, specified as True, or Logic 1. Thus, if any input (I1 OR I2 OR I3) is True (0V), then the output (O1) is True.

While the action of the gate has been explained on the basis of -12 volts as a False input for I1, I2, and I3, in practice, the inputs will be somewhat less, about -8 volts. However, this in no way changes the logic action of the gate because the output (O1) will simply be the least negative of the inputs when all are False, which still means a False output that is more negative than 0V. And, when any input is True (0 volts) it makes no difference whether the other inputs are -12 volts or -8 volts since the output (O1) will be 0 volts.



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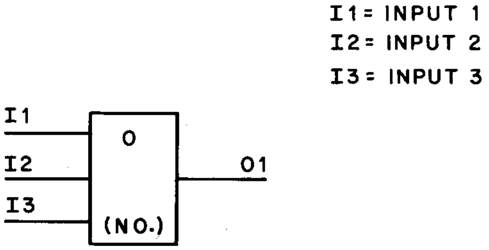


LOGIC SYMBOL

While the action of the diode when conducting is to allow current to flow through the load (R) which causes the change of voltage at the output, it is a useful convention to think of the diode as a short circuit when conducting, thus the 0 volts at the anode of D1 appears at the cathode and O1 becomes 0 volts.

At an OR gate, if ANY input (I1, or I2, or I3) goes True (0) the output goes True, hence the name (+) OR. Conversely, if ALL inputs are False, then the output is False, and this configuration can be called a negative (-) AND gate.

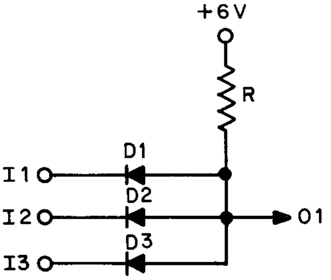
2. AND GATE

A diode (+) AND gate is quite similar to an (+) OR gate except that the diode connections are reversed and the bias is opposite, as shown.

If I1 AND I2 AND I3 are all True (0 volts), then all diodes are forward biased, the diode current through R drops all the +6 volts, and O1 is True (0 volts). Thus, the configuration is called an (+) AND. However, assume I1 goes to -12 volts. D1 conducts more heavily because of the total of 18 volts (+6 to -12) applied. In effect, the anode of D1 becomes -12, thus O1 goes to -12 (False). This -12 volts also back-biases D2 and D3, and effectively they are no longer in the circuit.

At an AND gate, if ALL inputs are True, the output is True, hence the name (+) AND. Conversely, if ANY input is False, the output is False and this configuration can be called a negative (-) OR.

It is important to remember that the inputs to a gate determine the output and a +OR can act as a -AND. Conversely, a +AND can act as a -OR. A useful way to determine the effect of a gate, however named, is to determine the logic level required at the output, and then determine the logic level of the input signals necessary for that output.



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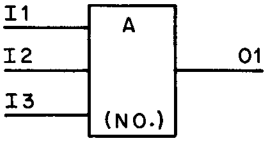


LOGIC SYMBOL

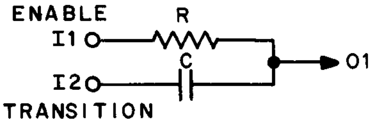
I1 = INPUT 1
I2 = INPUT 2
I3 = INPUT 3

3. AC GATE

A special AND gate configuration is called an AC gate to specifically denote that the valid output is caused by a False to True (+) transition. The leading (and trailing) edge of a pulse waveform is considered to contain the high frequency components, thus a gate which is operated by the leading edge of a pulse can be named for clarity as an AC gate.

An AC gate is composed of a resistor-capacitor combination as shown below.

The resistor input, I1 in this case, is called the Enable, sometimes referred to as the permit (or permiss) side of the gate. The True transition is applied to the capacitor side of the gate. The ◇ in logic symbology denotes a capacitor.



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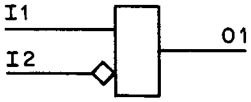
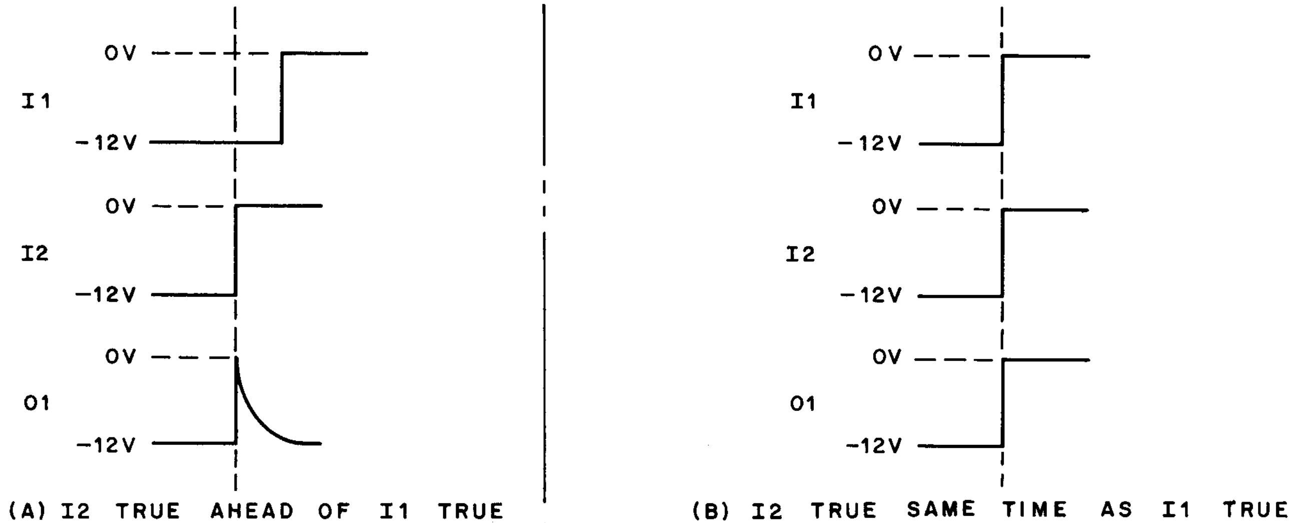
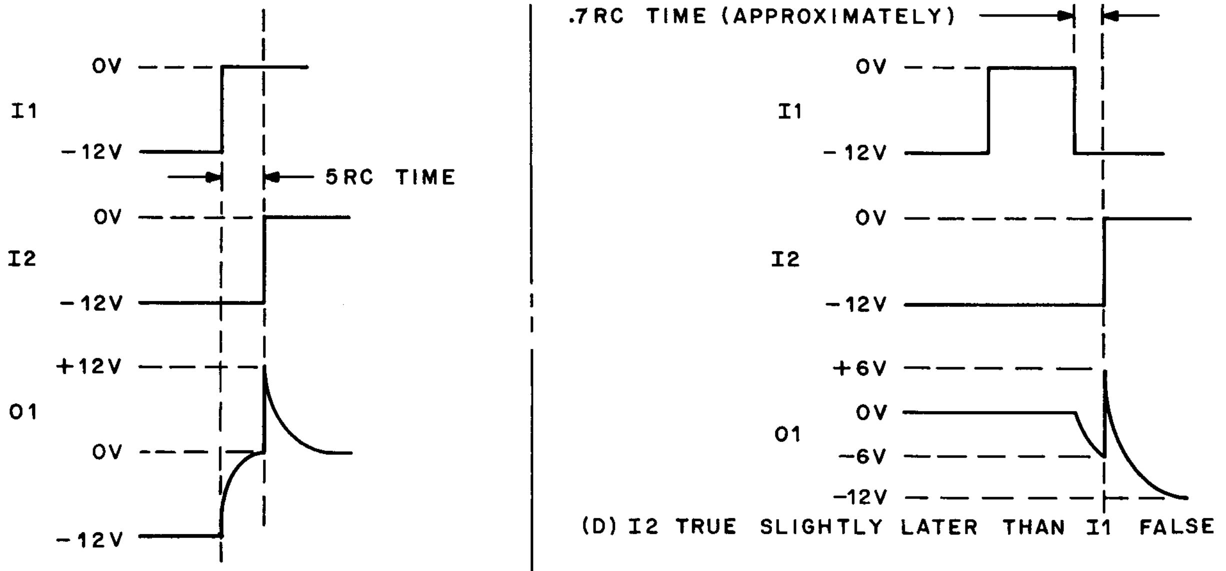


LOGIC SYMBOL



(A) I2 TRUE AHEAD OF I1 TRUE

(B) I2 TRUE SAME TIME AS I1 TRUE



(D) I2 TRUE SLIGHTLY LATER THAN I1 FALSE

(C) I2 TRUE LATER THAN I1 TRUE

Figure 2-20. AC Gate Waveforms

As illustrated by the waveforms (Figure 2-20) there are four specific conditions of importance to the understanding of the action of the gate. The gate will be explained from an initial condition of both inputs False (-12). Thus, C has no charge, since both sides are equal and of the same polarity, and 01 is -12 through R connection.

In condition (A), assume I2 goes True (0V), with I1 at -12. C must now charge to -12 volts on I1 side, and the charge current through R drops all the -12 volts and 01 instantaneously goes to 0, then to -12 at an RC rate. It is a useful convention to think of C as being a short circuit to a fast change of voltage, thus the 0 volts applied to I2 immediately appears at 01 side through C. Therefore, when I2 goes True (0), 01 goes True. This is not a valid transition since 01 must go positive with respect to ground, and 01 only reached ground, and did not go above.

In condition B, both I1 and I2 go True (0V) simultaneously. Since both sides of C remain at the same polarity with respect to each other, there is no change of charge, and O1 goes True (+AND) since both inputs go True. This, again, is not a valid transition since O1 does not go + with respect to ground.

In condition C, I1 goes True (0V) ahead of I2. At the time of I1, then, I2 is at -12 (False), and C charges to -12 on I2 side (0 on I1 side). Assume the time is long enough (5RC time) for C to have charged. Now, when I2 goes True (0V), C must discharge through R. Discharge current is maximum at the first instant and the voltage across R is maximum (12 volts) and in a polarity that makes O1 positive with respect to ground, and this is a valid transition.

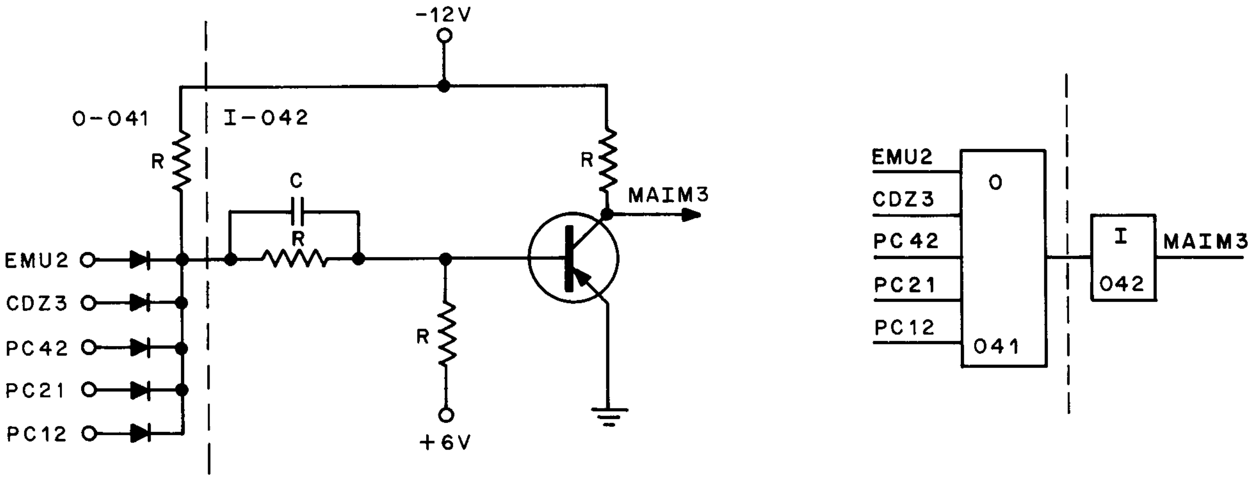
In condition D, I1 goes False and I2 goes True slightly later than I1. During the time I1 was True, I2 was False and C became charged to -12 on I2 side. Now I1 goes False and C starts to discharge across R in a polarity to make O1 go in a negative direction. Before C can change very much because of R in the discharge path, and become very negative, I2 goes True. What is left of the charge on C will appear at the first instant across R in a polarity that will make O1 positive. As illustrated, enough time difference is between I1 and I2 to allow C to lose 6 volts of charge. However, when I2 goes True, the 6 volts left on C appears at O1 as positive with respect to ground and is a valid transition.

One of the main uses of an AC gate is to trigger a FF into a specific condition of set or reset. (See FF discussion for fuller explanation.) Refer to Lesson 20 of Electronic Course for further information on Logic Gates.

4. LOGIC NETWORKS

A logic network (net) is a logic configuration in which the named output is either a logic 1 or a logic 0, depending on the logic design. A positive net in the EC-130 logic is defined as one in which the named output is logic 1. A negative net is one in which the output is logic 0. The EC-130 is described in terms of positive nets in the Computer Printout (MDD). (See Figure 2-21.)

O-041 together with I-042 constitute a positive net. By definition MAIM3 must be True, therefore the input to I-042 must be False. Since O-041 is an OR gate, if any input is True, the output is True at I-042, and inverted by I-042, will be False. This is not a valid output by definition. In order that the output of O-041 be False, all inputs must be False. Therefore, O-041 must act as a -AND to fulfill the logic requirement that MAIM3 be True at the output of I-042. It has been previously explained that a + OR and a -AND are the same configuration and the inputs decide the output (See OR gate discussion.)



SCHEMATIC LOGIC SYMBOL

Figure 2-21. Logic Network

5. LOGIC EQUATIONS

In the Computer Printout developed as part of the documentation of the EC-130 a logic equation is a word description using Boolean algebra in a form of "Modified Polish Notation" that specifically delineates any named signal in the positive net logic design. As an example, using MAIM3, the logic equation reads:

This logic equation states: EPC4 FF reset output (PC42), EPC2 FF set output (PC21), EPC1 FF reset output (PC12), Multiply FF reset output (EMU2), and D Counter zero (gate) output (CDZ3) when OR'd together will give a specific output that will be False when all inputs are False. This False output, inverted True by I-042 (designated by the apostrophe ('')), will be MAIM3 True signal, which will fulfill the logic requirements as specified by the logic design.

```
( PC42    PC21    PC12    EMU2    CDZ3  + ) '
```

F. BASIC TIMING

The timing element in the EC-130 is the frequency of the oscillator, which is nominally 666 KC. Small variations of oscillator frequency have no significance because the timing chain and the data sequence are re-synchronized at the end of each Home time.

1. OSCILLATOR

The oscillator (Figure 2-22) is a typical colpitts, which can be recognized by the tapped-capacitor feedback voltage divider across the resonant tank circuit. This type of Oscillator is covered in Lesson 19 of Friden Electronic Course. One untypical characteristic of the oscillator in the EC-130 is excessive feedback, which gives an unsymmetrical output waveform. This is of no consequence since only a portion of the waveform is used.

The waveform across the emitter of Q1 is applied to the base of Q2, which is connected as an emitter-follower. As the waveform at the base of Q2 goes more positive, the emitter of Q2 goes more positive. This positive going change is felt immediately at the base of Q3 through the 68 Pf speed-up capacitor and 1.5 K resistor. Q3 cuts off when this waveform reaches a level that overcomes the negative base bias. When Q3 cuts off, Q3 collector goes to -12 volts, and remains at -12 V until the waveform at the base of Q3 decreases to a level that permits the negative bias to turn Q3 on again. When Q3 turns on, Q3 collector goes essentially to ground (0 Volts).

The output is taken from the collector of Q3 and is essentially a square wave that varies from 0 Volts to -12 Volts with each oscillator alternation. The output of the oscillator circuit is designated TOSC4 (Timing, Oscillator, Inverted False) and is used to control the output of OR gate O-168 acting as a negative AND. The other input to O-168 is HOME1 (Home FF Set output), which will be False (-12 Volts) when Home FF is in reset condition. The action of O-168 on the timing chain will be covered as applicable.

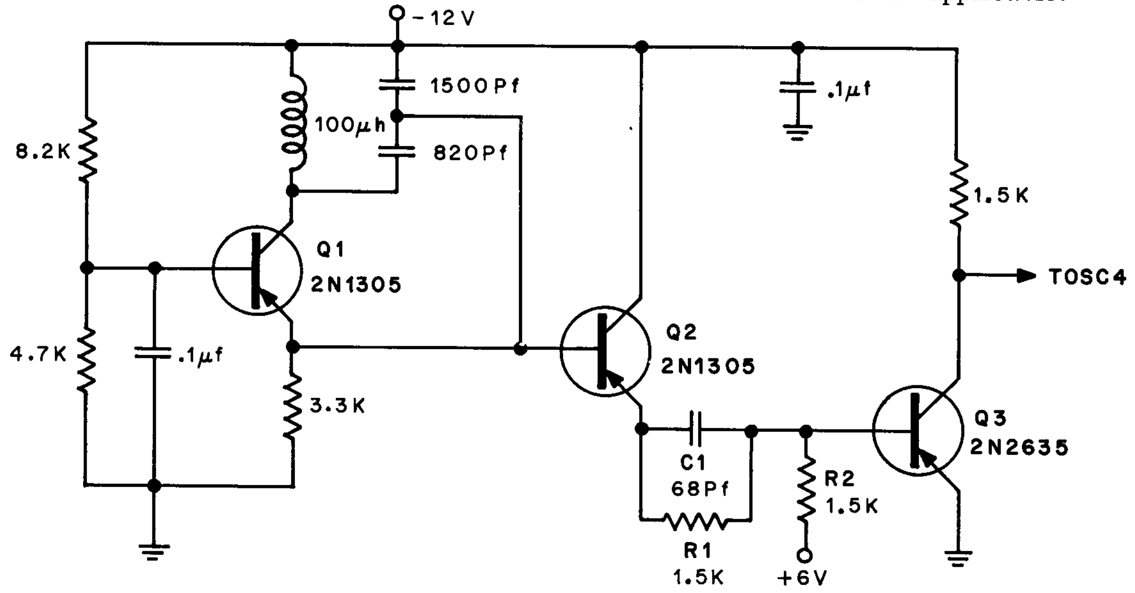


Figure 2-22. Master Oscillator Schematic

2. MACHINE START

When the machine is first turned on, the application of the +6 and -12 power supply outputs across the zener-voltage-divider sets Start FF. (See Figure 2-23.) The reset output of Start FF (ESTA2) is False and is inverted to True by I-001, the output of which is designated ESTA3.

ESTA3 True applied through a diode to the reset side of Home FF clamps the FF to reset condition. HOME2 is True, and HOME1 is False. The Oscillator output (TOSC4) and HOME1 are inputs to gate O-168 acting as a -AND. The output of O-168 will go False with each oscillator alternation as long as HOME1 is False. The output of O-168 is inverted True by I-169, designated TOSC3, and is applied as a transition signal to the T-input of Clock FF. TCLK2 output of the Clock FF will go True every other oscillator transition and is used to trigger the timing chain at a 333 KC rate, or, in other words, the output frequency of the oscillator divided by two.

Action of the Timing Chain will cause a set to reset transition of L FF at specific intervals. L FF reset output (TFL2) False to True transition is applied to the set input of Home FF. However, as long as the reset side is clamped reset by ESTA3 being True, TFL2 transition cannot set Home FF. ESTA3 will not go False until Start FF is reset, and therefore the timing chain, which has been started by the turning on of the machine, will run continuously until Start FF resets.

3. FUNCTION START

The first function or Digit Entry at the keyboard initiates keyboard delay (EKBD3) which is applied as an input to the reset side of Start FF. EKBD3 + transition resets Start FF and the FF will remain reset. When reset output (ESTA2) goes True, ESTA2 inverted by I-001 goes False (ESTA3) and removes the clamp on the reset side of Home FF. With the clamp removed, the next TFL2 transition from the timing chain will set Home FF. The set output of Home FF (HOME1) goes True and inhibits gate O-168. The oscillator transition can no longer trigger Clock Control FF and the timing chain stops, but at a predetermined setting which will be covered in Timing Chain discussion.

a. SYNC PULSE. Reset of Start FF, in addition to stopping the timing chain, places a pulse into the delay line, designated Sync pulse, previously called Start pulse. The first pulse off the delay line, then, will be this Sync pulse. This Sync pulse off the delay line, in addition to being sent through the counters, is also applied to the reset side of Home FF (as CIA9) and will reset Home FF. Reset of Home FF causes HOME1 to go False and this signal enables gate O-168 and permits the oscillator output to trigger the Clock FF.

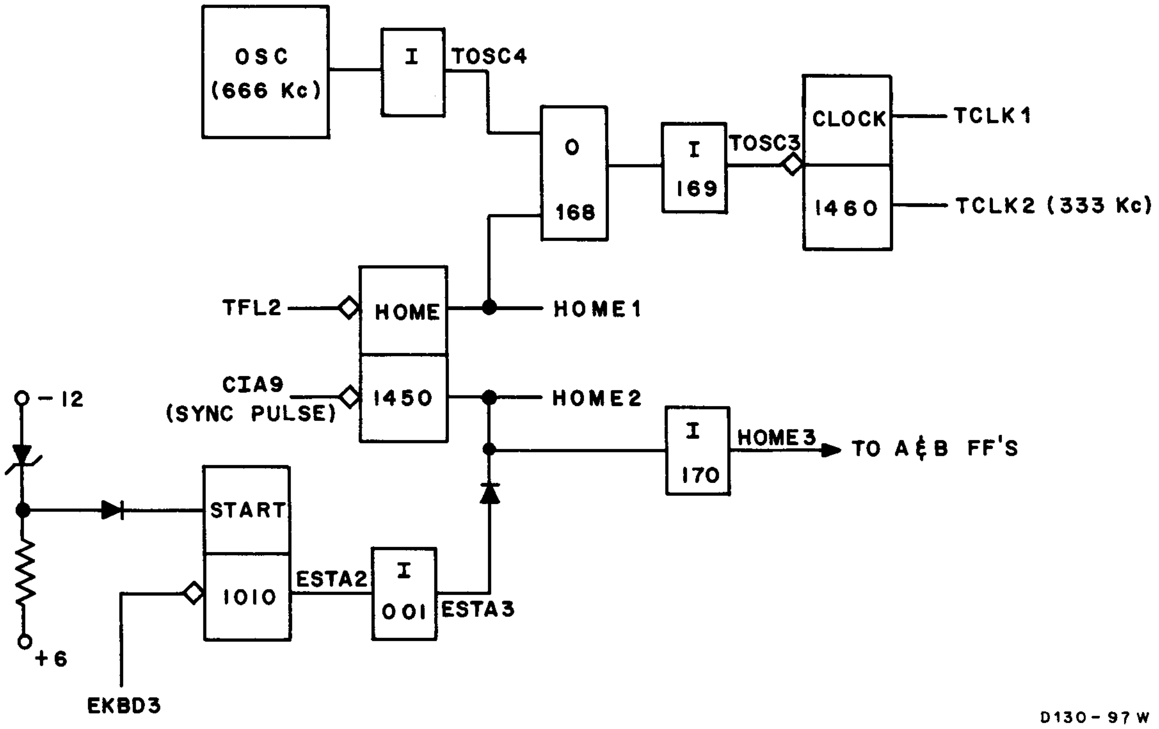


Figure 2-23. Start Logic

The result of the sequence of events discussed is that turning on the EC-130 starts the timing chain, which will run continuously until a function or Digit Entry is initiated at the keyboard, which in turn initiates "keyboard delay". Keyboard delay (EKBD3) resets Start FF, which enables TFL2 to set Home FF. Home FF being set inhibits the input of the Oscillator to the Timing Chain by inhibiting gate O-168. Turning on the EC-130 also places a Sync pulse on the delay line. This Sync pulse, when it comes off the delay line, is applied to reset Home FF which, in turn, enables gate O-168 and permits the Oscillator to trigger the Timing Chain. At some future time, less than 4.32 ms, TFL2 goes True and sets Home FF which inhibits gate O-168 until the Sync pulse again comes off the delay line and starts the sequence over again. Thus, the Sync pulse from the delay line starts the timing chain on each trip off the line. If the Oscillator frequency should change slightly, or the time of delay on the delay line should change, it would be of no consequence because the data and the timing chain are re-synchronized each trip through the line.

4. BIT COUNTER

The Bit Time Counter is a group of four-flip-flops so interconnected as to give a basic count of 16. In other words, it will take 16 pulses into the counter to get a + transition signal at the output of D FF (TFD2), which is the end FF of the four FF's.

Reference to the Truth Table (See Figure 2-24) shows that the first count is initiated at a preset condition of 3; meaning A is set, B is set, and C and D reset. This is accomplished by using the reset output, designated HOME2, of Home FF, which will go False when Home FF sets. When HOME2 goes False, the False is inverted to True by I-170, designated HOME3, and applied to the set side (collectors) of both A and B FF's, which clamps A and B to "set" condition, by definition, B3 time. The first pulse in, then, from Clock FF (TCLK2) will reset A. Reset of A gives a + transition (TFA2) which resets B. Reset of B gives a + transition (TFB2) which sets C. Set of C will not give the necessary + transition (TFC2) to set D, therefore, the result of this first pulse input is: A reset, B reset, C set, D reset, which is a count of 4. The next pulse in then sets the chain to 5, and so on.

Once, however, that the counter is started, the Bit Counter will count through fifteen and start over each time as long as TCLK2 True pulses are permitted into A FF by the action of O-168 on the clock FF T-input.

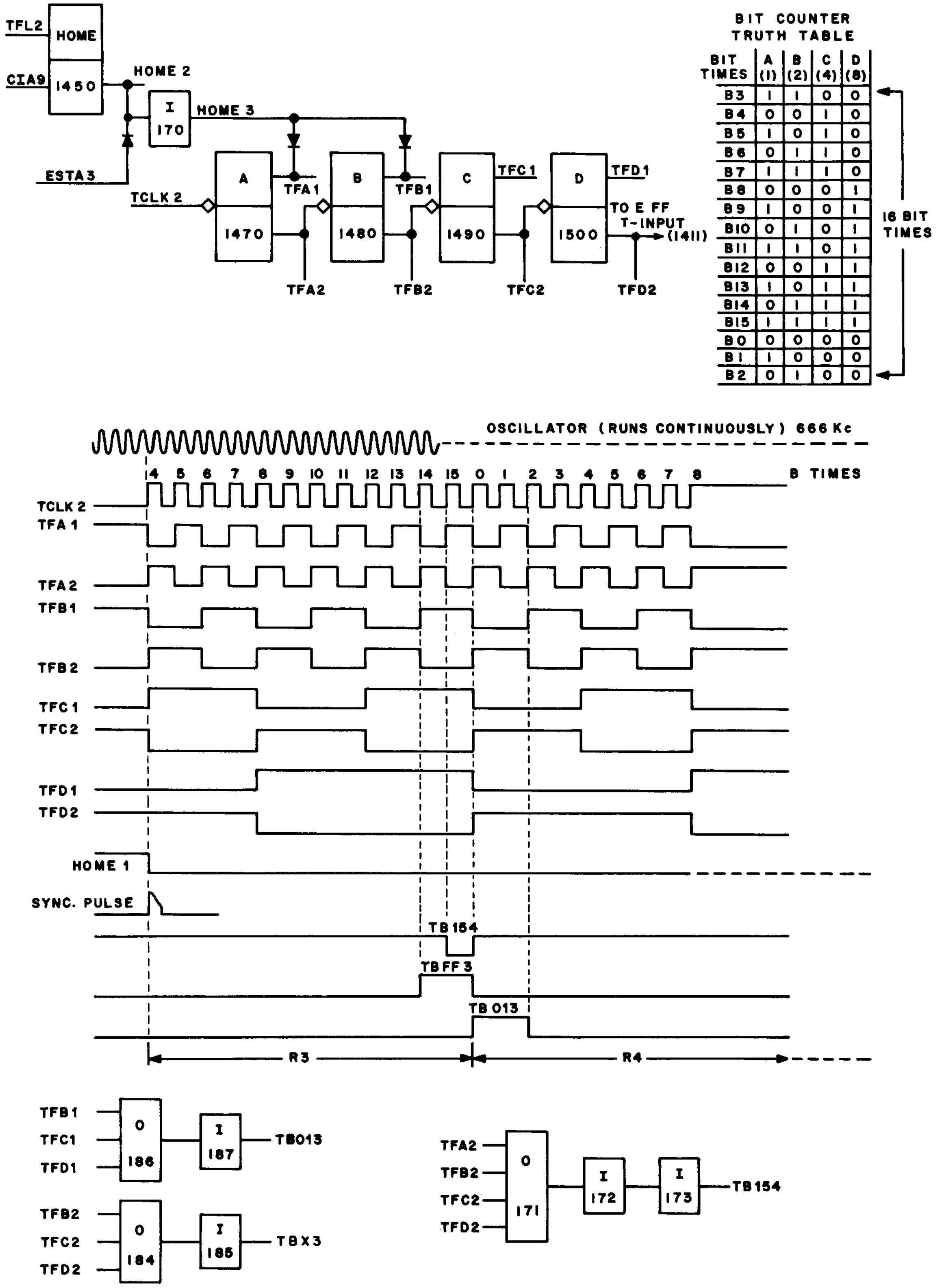
Logic control in the EC-130 requires that timing signals be available at specific times which are delineated by Bit Counter FF settings. These times are derived from specific Bit Counter FF outputs gated together and inverted. The three specific times developed are: B0 (or) B1 time (TB013), B14 (or) B15 time (TBX3), and B15 time False (TB154). All of these times are used in the control logic.

B0 (or) B1 time is developed by inverter I-187 controlled by gate O-186 acting as a -AND. Reference to the waveforms for the Bit counter shows that only at B0 and B1 time are set outputs from FF's B, C, and D False (B reset, C reset, and D reset). When all inputs to O-186 are False, the output is False. The output of O-186 is inverted True by I-187, and will be True only during that period of time that TFB1, TFC1, TFD1 are False, and this is defined as B0 (or) B1 time. Reference to the Truth Table shows that the count in the Bit Counter specifies B0 or B1 at this time. The output of I-187 is designated TB013.

B14 (or) B15 time is developed by inverter I-185 controlled by gate O-184 acting as a -AND. Reference to the waveforms for the Bit Counter shows that only at B14 or B15 times are reset outputs from FF's B, C, and D False. When all inputs to O-184 are False, the output is False. The output of O-184 is inverted True by I-185, and will be True only during that period of time that TFB2, TFC2 and TFD2 are False (B set, C set and D set). This is defined as B14 (or) B15 time. Reference to the Truth Table shows that the count in the Bit Counter is B14 or B15 at this time. The output of I-185 is designated TBX3.

B15 time False, designated TB154, is an extensively used signal and is specifically used to designate the end of a Register time, which is composed of 16 B times (B0 to B15). One use of TB154 is to designate the time that data is to be shifted between counters, which is at the end of each Register time.

TB154 is developed by inverters I-172 and I-173 controlled by gate O-171 acting as a -AND. Reference to the waveforms for the Bit Counter shows that only during B15 time will TFA2, TFB2, TFC2, and TFD2 be False (A set, B set, C set, and D set). When all inputs to O-171 are False, the output is False. This output, inverted twice, will go False at the beginning of each B15 time. TB154 is used as an input to gates which are enabled by other signals that are long in comparison to TB154. The output of the gates when inverted can be used as a transition which occurs at the beginning of each B15 time.



BIT COUNTER TRUTH TABLE

BIT TIMES	A (1)	B (2)	C (4)	D (8)
B3	1	1	0	0
B4	0	0	1	0
B5	1	0	1	0
B6	0	1	1	0
B7	1	1	1	0
B8	0	0	0	1
B9	1	0	0	1
B10	0	1	0	1
B11	1	1	0	1
B12	0	0	1	1
B13	1	0	1	1
B14	0	1	1	1
B15	1	1	1	1
B0	0	0	0	0
B1	1	0	0	0
B2	0	1	0	0

D-130-98W

Figure 2-24. Bit Counter Logic

5. REGISTER COUNTER

The Register (R) Counter is a group of three (3) FF's (E, F, and G) interconnected to give a basic count of eight (8). (See Figure 2-25.) However, a special interconnection between G and F FF's inhibits two counts, so that the counter becomes a scale of six. This is sometimes called a "Permuted" counter. The count of six is specifically desired because the EC-130 has six register times that must be delineated for the operation of the machine logic.

At the beginning of Home time the last pulse, TFG2 (inverted to TGF3), that places all column counter FF's in the reset position (which is C0 time) will also leave Register counter FF's G and F set, and E FF reset. At the end of Home time, the Sync pulse from the delay line resets Home FF, whose reset output is designated HOME2. When Home FF resets, HOME2 goes True and is applied to reset side of G FF, which resets G. Reference to the Truth Table shows that E reset, F set, and G reset is the condition for R3. Since the established time of the Sync pulse is in C0R3 with respect to the timing chain, the register counter is synchronized to the Sync pulse R time and thus to the data on the delay line.

Meanwhile, the Bit Counter was preset to B3 and will count up through B15 of C0R3 time. The first + transition from the Bit Counter (TFD2) to the register counter occurs at the end of R3 time and will set E FF to designate that the count is now in R4 time. At the end of R4B15 time, the next + transition from the Bit Counter (TFD2) signifies that R4 is over and RS time should start. This pulse would normally reset E, which would reset F, which would set G. However, when G sets, TFG2 goes False and, inverted by I-205 to True, is applied to set side of F FF, which sets F. Thus, the Register Counter ends up with E reset, F set, and G set, which is the designation for RS. From this time on, TFD2 transitions will advance R Counter through R0, R1, R2, R3, R4 and, at the end of each R4 time, will set R Counter to the permuted setting, which is RS, and the count starts over.

Any R time, or combination of R times, may be selected by using appropriate outputs from E, F, and G FF's. However, two specific R times are used in so many places that they are developed by gates and used to control inverters which will give necessary polarities. The two R times specifically developed are R0 and R1.

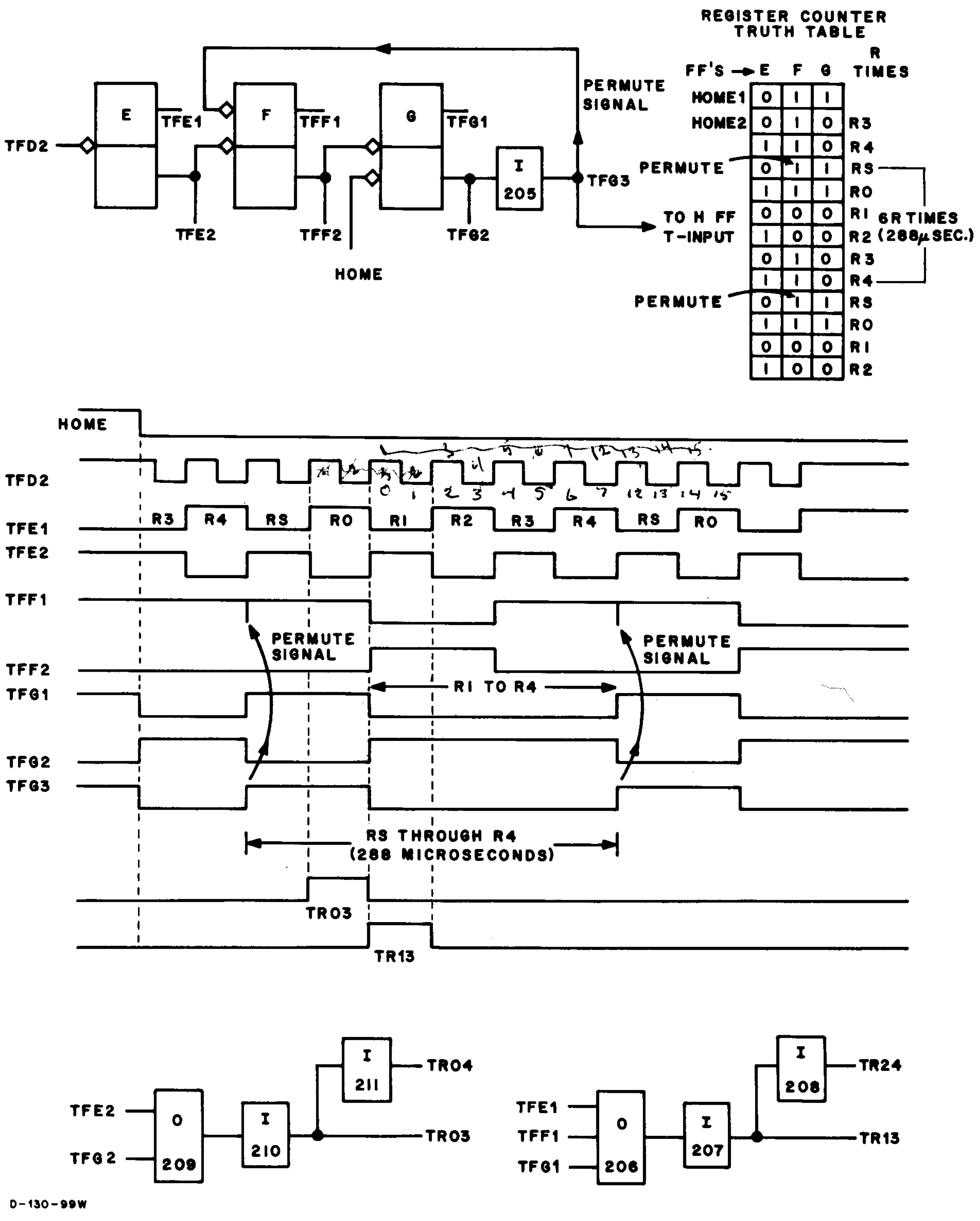
R0 time is developed by I-210 controlled by gate O-209 acting as a -AND. When TFE2 and TFG2 are both False, which will be only during R0 time, the output of O-209 will be False. O-209 output inverted True by I-210, designated TRO3, will be True during, and only during, R0 time. Inverter I-211 inverts the output of I-210 for polarity purposes. The output of I-211 will be False during R0 time, designated TRO4, and is used as an input to gates for logic purposes when a False at R0 time is desired.

R1 time is developed by I-207 controlled by gate O-206 acting as a -AND. When TFE1, TFF1, and TFG1 are all False, which will be only during R1 time, the output of O-206 will be False. O-206 output inverted True by I-207, designated TR13, will be True during, and only during, R1 time. I-208 inverts the output of I-207 for polarity purposes. The output of I-208, designated TR14, will be False during R1 time and is used as an input to gates for logic purposes when a False signal at R1 time is desired.

6. COLUMN COUNTER

The Column (C) Counter is a group of four FF's (H, J, K, and L) interconnected to give a count of sixteen (16). (See Figure 2-26.) While there are 16 column times in the EC-130, only C1 to C14 are used for display. However, some arithmetic operations require use of C15 time in the logic. The 16th column time, C0, is of an indeterminate time because it consists of the time existing after C15 time and before C1 time begins again. This time is the delay line time (approximately 5000 usec) less one timing chain cycle (4320 µsec). This is because at the end of C15 time (the beginning of C0 time) TFL2 stops the input to the Clock FF at gate O-168 by setting Home FF and C0 time cannot end until the Sync pulse comes off the delay line and resets Home. At the end of C15 time the timing chain is stopped because no Clock FF input is permitted, then, after a period of time that is a function of the actual travel time of the delay line, Sync pulse enables the Clock FF input to the timing chain, which has been preset, and the count starts over and will be in synchronization with the data as it comes off the delay line.

The column counter is a typical scale of 16 counter which counts down the input (TFG2 inverted to TFG3) by sixteen (16). TFG2 denotes the end of each group of six register times and the settings of the column counter FF's denotes the column times. The column counter will advance one column time for each TFG2 transition. At the end of 16 TFG2 transitions, all FF's (H, J, K, and L) are reset and TFL2 output, which transitions False to True, is used to set Home FF. Setting of Home FF inhibits gate O-168 because HOME1 goes True, and the Oscillator input to Clock FF is inhibited. Therefore there is no input to the timing chain; the column counter FF's remain reset; and all FF's in the chain remain in their last state ex-



REGISTER COUNTER TRUTH TABLE

FF'S →	E	F	G	R TIMES
HOME1	0	1	1	
HOME2	0	1	0	R3
	1	1	0	R4
PERMUTE	0	1	1	RS
	1	1	1	R0
	0	0	0	R1
	1	0	0	R2
	0	1	0	R3
	1	1	0	R4
PERMUTE	0	1	1	RS
	1	1	1	R0
	0	0	0	R1
	1	0	0	R2

6R TIMES (288μSEC.)

D-130-99W

Figure 2-25. Register Counter Logic

cept FF's A and B. Set of Oscillator Control FF makes HOME2 False, and HOME2, inverted True by I-170, is used to preset Bit Counter FF's A and B (See Bit Counter discussion). This condition remains until the Sync pulse comes off the delay line and resets Home FF. Reset of Home FF makes HOME2 True, which is applied in the Register Counter to establish the preset condition of F and G FF's (See R counter discussion). At the same time, HOME1 goes False and is applied to enable gate O-168, which enables the Oscillator input to Clock FF, which in turn starts the timing chain from the preset conditions. The count continues until TFL2 goes True again and starts the timing sequence over. This timing sequence occurs continuously from the time the first function or Digit Entry is initiated at the keyboard and puts Sync pulse on the delay line.

Any C time, or combination of C times, may be selected by using appropriate outputs from the H, J, K, and L FF's. However, specific C times that are used in many places are delineated by gates and used to control inverters that give necessary polarities. The C times specifically developed are: C0, C1, C2, C15, and a complex signal designated TCX5.

C0 time, designated TC03, is developed by I-220 controlled by gate O-219 acting as a -AND. When TFH1, TFJ1, TFK1, and TFL1 inputs are False, which will be only during C0 time (all FF's reset - See Truth Table and Waveform Chart), the output of O-219 will be False. O-219 False output inverted by I-220 will be True and is specified as C0 time.

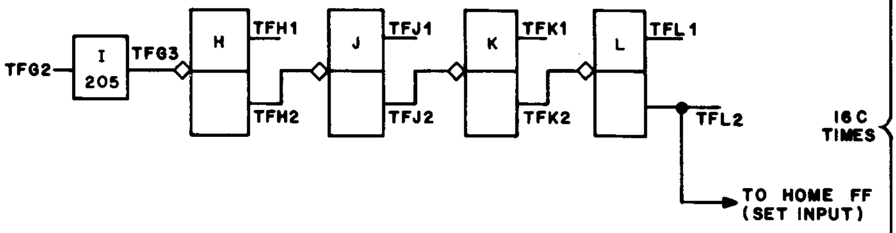
C1 time, designated TC13, is developed by I-213 controlled by O-212 acting as a -AND. When TFH2, TFJ1, TFK1 and TFL1 inputs are False, which will be only during C1 time (H set, and J, K, L reset - See Truth Table and Waveform Chart), the output of O-212 will be False. O-212 False output inverted by I-213 will be True and is specified as C1 time. For logic purposes, the output of I-213 is inverted False by I-214, designated TC14, and is used to specify C1 time at gates where a False is needed at C1 time.

C2 time, designated TC23, is developed by I-216 controlled by gate O-215 acting as a -AND. When TFH1, TFJ2, TFK1, and TFL1 inputs are False, which will be only during C2 time (See Truth Table and Waveform Chart), the output of O-215 will be False. O-215 False output inverted by I-216 will be True, and is specified as C2 time. For logic purposes, the output of I-216 is inverted by I-228 to False, designated TC24, and is used to specify C2 time at gates where a False is needed at C2 time.

C15 time, designated TC153, is developed by I-230 controlled by gate O-229 acting as a -AND. When TFH2, TFJ2, TFK2, and TFL2 inputs are False, which will be only during C15 time (See Truth Table and Waveform Chart), the output of O-229 will be False. O-229 False output inverted by I-230 will be True and is specified as C15 time. For logic purposes, the output of I-230 is inverted by I-231 to False, designated TC154, and is used to specify C15 time at gates where a False is needed at C15 time.

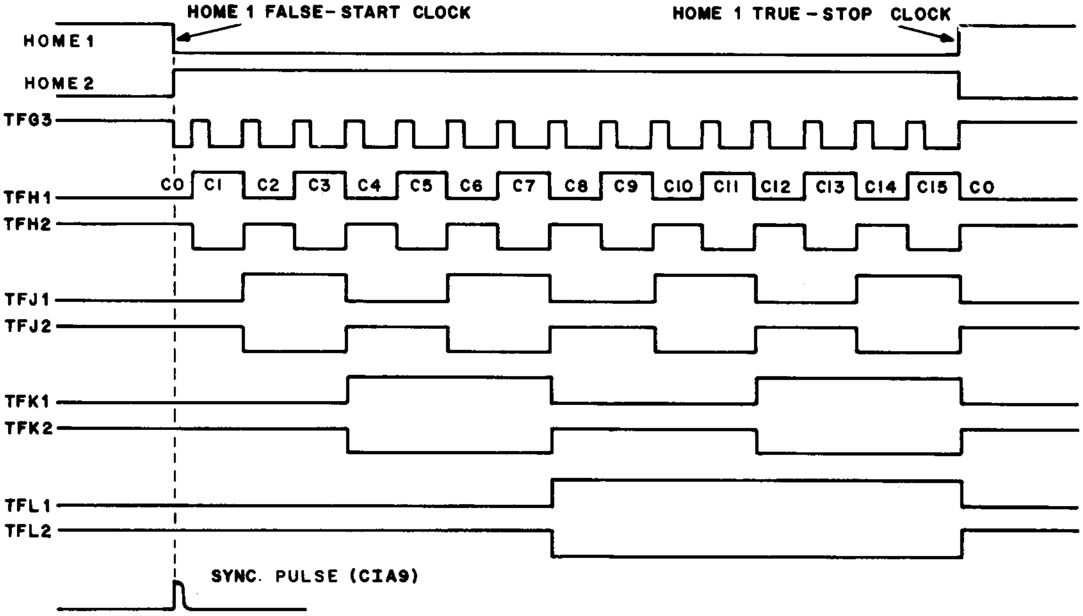
C0 time is not used in a function, C15 time is used only in a divide function, and C1 is reserved for the algebraic sign of a register. However, these terms are combined in a complex expression, designated TCX5, by means of gates and inverters and used for machine logic functions. The expression TCX5 is developed by gate O-600. The inputs to O-600 are developed by I-218 and I-233. I-218 output, designated TC013, is controlled by O-217 acting as a -AND. When TFJ1, TFK1, and TFL1 inputs are False, which will be only during C0 or C1 time, the output of O-217 is False and, inverted True by I-218, is used to specify C0 or C1 time. I-233 output is controlled by O-232 acting as a -AND. The two inputs to O-232 are TC154 and EDV1. When TC154 is False, which will be during C15 time, and EDV1 is False, which will be in any function other than Divide, the output of O-232 will be False. O-232 output inverted by I-233 will be True during C15 except in a Divide function.

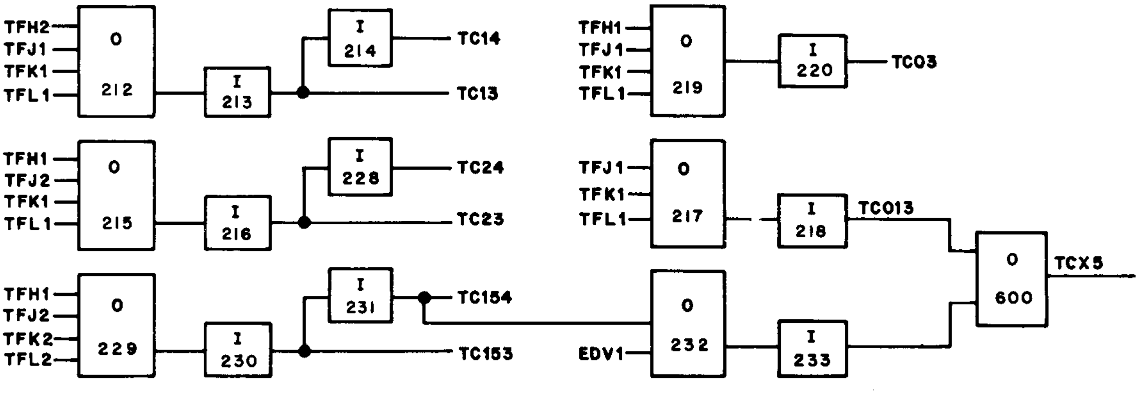
Of course, the reverse of the above explained action of the gates can be true in that, if all polarities of inputs are reversed, then O-600 will act as a -AND, and the output will be False from C2 through C14 time, except in Divide. In Divide, the output of O-600 will be False from C2 through C15 time.



16C TIMES

(1) H	(2) J	(4) K	(8) L	
0	0	0	0	C0
1	0	0	0	C1
0	1	0	0	C2
1	1	0	0	C3
0	0	1	0	C4
1	0	1	0	C5
0	1	1	0	C6
1	1	1	0	C7
0	0	0	1	C8
1	0	0	1	C9
0	1	0	1	C10
1	1	0	1	C11
0	0	1	1	C12
1	0	1	1	C13
0	1	1	1	C14
1	1	1	1	C15





D-130-100W

Figure 2-26. Column Counter Logic

G. LOGIC CONTROL

A function in the EC-130 is a series of orderly progressions of logic actions. A series of logic actions that perform specific data handling or arithmetic operations within a logic loop are specified as Entry Phase Counter (EPC) steps. These steps are defined by the specific settings of a group of three FF's designated as the Entry Phase Counter.

Decimal alignment of the numbers in the EC-130 is controlled by a group of four FF's designated as the Decimal Point Counter (DPC). The DPC also controls logic actions that develop the arithmetic answer.

1. ENTRY PHASE COUNTER (EPC)

The EPC is a group of three (3) FF's connected to give a total binary count of 8, 0 through 7. (See Figure 2-27.) Reference to the Function Flow Charts in Function Logic discussion shows that logic actions are specified by specifically designated numbered settings of the EPC. Certain of the major settings of the EPC that occur, some of which are outside of the normal binary progression, are discussed as follows.

a. UNCLAMP EPC. At the end of any function and during Idle, EPC becomes clamped to Zero. The first action in any function is to unclamp EPC. This is controlled by O-016. The inputs to O-016 specify Common Digit FF set (ECD1 True) or Common Function FF set (ECF1 True). If either input to O-016 is True, the output is True. True output of O-016 is inverted False by I-017, designated ECFD4. ECFD4 when True clamps reset outputs of all EPC FF's to True through isolation diodes. Therefore, when ECFD4 is False, EPC FF's are no longer clamped reset, and EPC is free to be stepped off Zero. Step of EPC is designated "increment EPC".

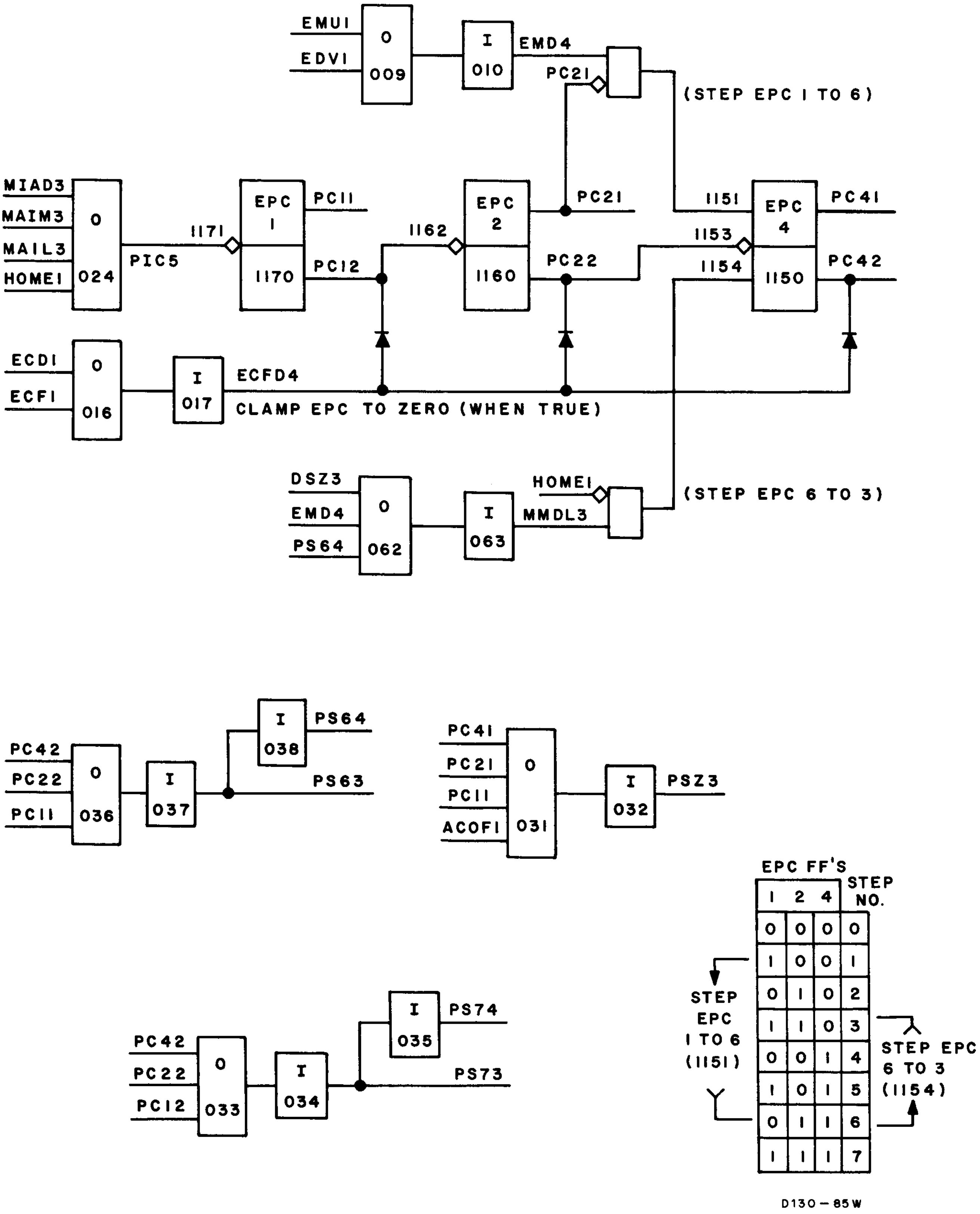
b. INCREMENT EPC. Increment EPC is controlled by O-024. The logic construction of O-024 specifies that when all inputs are False and then one goes True, the output transitions False to True. The output of O-024 is designated PIC5 (Increment EPC, True). The increment signal is Home 1, which goes False to True at the end of each data sequence (word time). The other signals on O-024 are inhibiting signals to prevent step of EPC when logic action requires more than one data sequence to complete. When any one of these inhibit signals is already True, then change of Home 1 from False to True can have no effect at the output, and EPC remains on that particular step until the particular inhibiting True signal goes False. PIC5 True is applied to capacitors at the T-input of EPC1 FF, and changes the state of EPC1 from set to reset, or vice-versa, depending on EPC1 FF state when PIC5 goes True. (See Basic Circuits discussion.) Change of state of EPC1 FF steps EPC up by 1 in an orderly progression as defined by the Truth Table. However, at certain points in the logic loops the logic requires that EPC revert to a previous EPC step, or requires a jump past certain EPC steps.

c. STEP EPC 1 to 6. At the end of EPC step 1 in every function except Multiply and Divide the logic requirement is that EPC step directly to 6 and bypass EPC settings 2, 3, 4, and 5.

Step 1 to 6 is controlled by O-009. If Mult and Div FF's are both reset (EMU1 and EDV1 False), the output of O-009 will be False, and inverted True by I-010, designated EMD4, enables an AC gate at the set input of EPC4 FF. EPC step 1 specifies EPC1 set, EPC2 reset, EPC4 reset (see Truth Table). The next PIC5 would reset EPC1, which in turn would set EPC2 with EPC4 remaining reset, specifying EPC step 2. However, when EPC2 sets, set output (PC21) goes False to True and provides a positive transition to the AC gate on EPC4 which is enabled by EMD4 True, and sets EPC4. EPC ends up with EPC1 reset, EPC2 set, and EPC4 set, which specifies EPC step 6. Thus EPC steps from 1 to 6 instead of from 1 to 2.

d. STEP EPC 6 to 3. During the arithmetic of Multiply and Divide functions, logic requirement may specify step of EPC from 6 to 3 instead of 6 to 7.

Step 6 to 3 is controlled by O-062. If function is Multiply or Divide, EMD4 will be False at O-062. If the arithmetic logic is not complete, DSZ3 at O-062 will be False. During EPC step 6, PS64 will be False at O-062. When all inputs to O-062 are False, the output is False, and is inverted True by I-063, designated MMDL3. MMDL3 True enables an AC gate at reset input of EPC4 FF. EPC step 6 specifies EPC1 reset, EPC2 set, and EPC4 set. The next PIC5 (caused by HOME1) would set EPC1 and all FF's would be set, specifying EPC step 7. However, the same positive transition (HOME1) that would place EPC1 to set condition is also applied to the AC gate enabled by MMDL3 at the reset input of EPC4, and resets EPC4. EPC ends up with EPC1 set, EPC2 set, and EPC4 reset, which specifies EPC step 3. Thus EPC steps from 6 to 3 instead of from 6 to 7. The EPC jump from 6 to 3 is repeated each EPC6 time until the arithmetic of the problem is completed which is indicated by



EPC FF'S			STEP NO.
1	2	4	
0	0	0	0
1	0	0	1
0	1	0	2
1	1	0	3
0	0	1	4
1	0	1	5
0	1	1	6
1	1	1	7

Figure 2-27. Entry Phase Counter (EPC)

DSZ3 going True at O-062. When DSZ3 goes True, MMDL3 goes False, which no longer enables the AC gate on EPC4 FF reset input, and EPC steps 6 to 7.

e. CLAMP EPC to O. During any function either CD or CF is in set condition. At the end of the function, the CD or CF FF becomes reset, whichever is set, by PS73 and Home 1 at an AC gate common to reset inputs of both CF and CD FF's. When both CF and CD are reset, ECF1 and ECD1 are False at O-016, and O-016 output is False. O-016 False output is inverted True by I-017, designated ECFD4, and is applied through isolation diodes to the reset outputs of all EPC FF's. When ECFD4 is True, all EPC FF's are clamped to reset, which is specified as EPC Zero.

f. EPC LOGIC OUTPUTS. Any particular EPC step may be specified by set or reset outputs from applicable EPC FF's. However, certain EPC steps are used extensively so that they are delineated by logic gates which control inverters to give necessary logic polarities.

(1) EPC Step O. Reset condition of all EPC FF's, which is designated EPC O, is delineated by O-031. PC41, PC21, and PC11 will all be False at O-031 when EPC FF's are reset. ACOF1 will be False except under a special condition which is covered under Subtract Function discussion (See Function Logic). When all inputs to O-031 are False, output is False and is inverted True by I-032, designated PSZ3 ((Entry) Phase step Zero, True). Logic functions of PSZ3 are covered where applicable in specific function logic discussions.

(2) EPC Step 6. Development of EPC step 6 logic signal is controlled by O-036. PC42, PC22, and PC11 will all be False at O-036 during EPC step 6. When all inputs to O-036 are False, output is False and is inverted True by I-037, designated PS63 ((Entry) Phase step 6, True). PS63 True is inverted False by I-038, designated PS64, and is used at logic gates where a False is needed to specify EPC step 6 during logic operations.

(3) EPC Step 7. Development of EPC step 7 logic signal is controlled by O-033. PC42, PC22, and PC12 will all be False at O-033 during EPC step 7. When all inputs to O-033 are False, output is False and is inverted True by I-034, designated PS73 ((Entry) Phase Step 7, True). PS73 True is inverted False by I-035, designated PS74, and is used at logic gates where a False is needed to specify EPC step 7 during logic operations.

2. DECIMAL POINT COUNTER (DPC)

The Decimal Point switch controls the column position of the decimal point on the Display. Once the decimal position is chosen by the Decimal Point switch, the DPC is preset to control the placement of the number entered in Register one (R1) with respect to that position. This is called Decimal Align, and occurs as a part of EPC step 1 in the logic progression of all functions. (See Function Logic discussion.)

The decimal point counter is preset again in Multiply and Divide functions to delineate the progress of the arithmetic of the function. A final preset of DPC also occurs in Multiply and Divide function that specifies the decimal alignment of the answer. (See Multiply and Divide Function Logic discussions.)

The DPC is a group of four (4) FF's connected to give a binary count of sixteen (16). (See Figure 2-28.) The DPC is an "up counter" and the increment, or count, of DPC is by changing the state of DPC1 FF. When DPC1 FF changes state, the effect on the other three FF's is as illustrated in the Truth Table. The specific states of the FF's can be used as a binary count that represents a number from 0 through 15 for a total of 16 counts.

a. INCREMENT DPC. The advance of DPC is controlled by O-059. The logic construction of O-059 specifies that when all inputs are False and then one of the inputs goes True, the output of O-059 transitions False to True, which is a positive transition, designated DIC5 (Increment DPC, True). DIC5 applied to the T-input of DPC1 FF causes DPC1 to change state from set to reset, or vice-versa. Each change of state of DPC1 FF causes a change in the DPC setting that corresponds to a binary count of 1 added to the previous setting, or, to state it differently, DPC is counted up by one.

b. DECIMAL ALIGN (EPC1) PRESET. When the Decimal Point switch is on a specific position, for instance 2, then certain of the AC gates at the set inputs of all DPC FF's are enabled through Decimal Point switch wafers E, F, G, and H. Then, when a positive transition is applied to the capacitor input of these AC gates, the enabled gates set the associated DPC FF's. Once the FF's are set, then advance, or count up, of DPC starts from this preset condition.

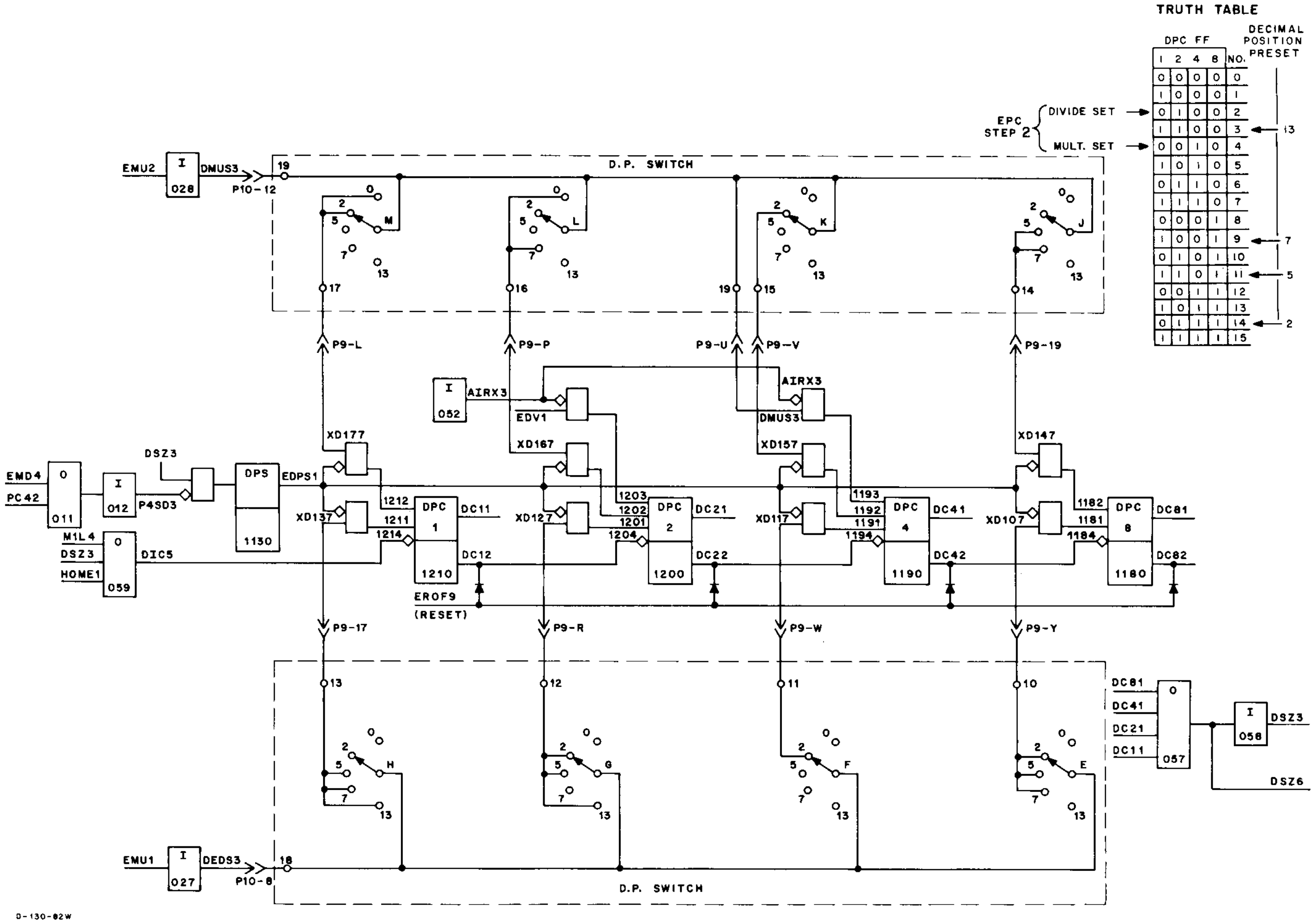
When the Decimal Position switch is on 2, the decimal point position indicates two columns to the right of the decimal point, meaning that the whole number portion of the entered number must be shifted two columns left to be in proper decimal position. These shifts left are controlled by DPC being set to 14, which means two more counts into DPC will bring DPC to zero. As illustrated, when the Decimal Point switch is on 2, DPC8, DPC4, and DPC2 FF set input AC gates are enabled by active connections on E, F, and G switch wafers.

The enable signal for Decimal Align is developed by I-027, designated DEDS3 (Entry or Divide set, True). The input to I-027 is the set output (EMU1) of Mult. FF, which will be False until Mult. FF is set. EMU1 False is inverted True by I-027 (DEDS3) and applied to E, F, G, and H switch wafers and enables those DPC AC gates actively connected through the wafers.

The signal that sets the DPC FF's that are enabled is the False to True transition of DPS FF set output (EDPS1), which occurs when DPS goes from reset to set condition. The logic of the setting of DPS FF will be covered as applicable in the Function Logic discussions.

c. MULTIPLY FUNCTION (EPC2) PRESET. Certain logic steps in a Multiply function are controlled by whether DPC is at zero, and, if not at zero, how many counts it takes to bring DPC to zero. In Multiply, the next set of DPC after Decimal Align is to a preset condition of 4, which means 12 more counts to bring DPC to zero.

This is accomplished by an AC gate at the set input of DPC4 FF that is enabled by reset output (EMU2) of Mult. FF inverted True by I-028, designated DMUS3. The output of I-052, designated AIRX3, goes False to True at EPC step 2 of Multiply (and Divide) and this transition is used at the enabled AC gate of DPC4 FF to set DPC4. Since DPC was counted to zero in EPC step 1 of Multiply (Decimal Align), the new condition of DPC with DPC4 set and all other FF's reset specifies a preset count of 4 in DPC, and it will take 12 more counts into DPC to bring DPC to zero.



TRUTH TABLE

EPC STEP 2	DPC FF 1	2	4	8	NO.	DECIMAL POSITION PRESET
	0	0	0	0	0	
	1	0	0	0	1	
DIVIDE SET →	0	1	0	0	2	
	1	1	0	0	3	← 13
MULT. SET →	0	0	1	0	4	
	1	0	1	0	5	
	0	1	1	0	6	
	1	1	1	0	7	
	0	0	0	1	8	
	1	0	0	1	9	← 7
	0	1	0	1	10	
	1	1	0	1	11	← 5
	0	0	1	1	12	
	1	0	1	1	13	
	0	1	1	1	14	← 2
	1	1	1	1	15	

Figure 2-28. Decimal Point Counter (DPC)

d. DIVIDE FUNCTION (EPC2) PRESET. As in Multiply preset, certain Divide logic steps are controlled by DPC. In Divide, however, the preset is to 2 instead of 4, which means 14 more counts into DPC to bring DPC to zero.

The preset to 2 is accomplished by an AC gate at set input of DPC2 FF which is enabled by set output (EDV1) of Divide FF, which will be True in Divide function. False to True transition of AIRX3 provides the transition in Divide that sets DPC2 FF. Since DPC was counted to zero in Divide EPC step 1 (Decimal Align), the new condition of DPC with DPC2 set and all other FF's reset specifies a preset count of 2 in DPC, and it will take 14 more counts into DPC to bring DPC to zero.

e. ANSWER ALIGN - MULTIPLY (EPC4) PRESET. In Multiply function, after the logic has developed the arithmetic answer, the number must be properly decimal aligned in R2. This is accomplished by setting the DPC to the 16's complement of the number of places to the left of the decimal position. For instance, if the column position of the decimal point indicates two places, there are 11 columns to the left of the decimal point and DPC sets to 5. The actual number set into DPC can easily be found by adding 3 to the decimal point position, therefore this method is indicated on the Flow Chart.

AC gates on the DPC FF's are enabled through switch wafers J, K, L, and M. The enable signal is developed by the reset output (EMU2) of Mult. FF inverted True by I-028, designated DMUS3. The transition signal is the set output (EDPS1) of DPS FF. In EPC step 1 of Multiply (and Divide) DPS becomes reset. In EPC step 4 of Multiply (and Divide) DPS is set again by the action of O-011. EMD4 is False at O-011 because function is Multiply, and PS42 will go False at EPC step 4. True to False output transition of O-111, inverted False to True by I-012, designated P4SD3, is applied to an AC gate at DPS FF set input. The enable on this gate is DPC zero (DSZ3), which will not be True until DPC has counted to zero from the preset count established in EPC step 2 of Multiply. When this DPS FF AC gate is enabled by DSZ3 being True, then the next P4SD3 (True) transition sets DPS, which in turn sets DPC for decimal alignment of the answer according to the position of Decimal Point switch.

f. ANSWER ALIGN - DIVIDE (EPC4) FUNCTION. In Divide function, the logic action that sets DPC for decimal alignment is very similar to the action in Multiply function. In Divide, the enable signal applied to the DPC AC gates is EMU1 False inverted True by I-027, designated DEDS3. DEDS3 True is applied through switch wafers E, F, G, and H, and enables DPC FF gates as specified by active connections on the switch wafers for a given decimal location. The transition signal that sets the DPC FF's is DPS set output (EDPS1) which transitions False to True. The logic of the DPS setting will be covered as applicable in Divide Function discussion.

For detailed explanations of the action of the DPC in particular functions refer to Function Logic discussion in this section of the manual.

H. FUNCTION LOGIC

Function Logic is a description by function of how the logic circuits of the EC-130 act to perform each specific function. The function explanations are related to Flow Charts for each function, and each Flow Chart is accompanied by a logic block diagram that specifies the logic gates involved in each EPC step. Each flow chart action is specifically delineated in the function logic explanation and referenced to the logic gates specified in the logic block diagram.

1. ADD FUNCTION

There is a distinction between an Add function chosen by pressing Add (+) key on the keyboard and internal "machine add". The internal machine decision to add or subtract is decided by comparing the algebraic signs of the two numbers as a part of the function. The machine may, on the basis of the algebraic signs, subtract in an add function, or add in a subtract function. The algebraic rules are: If the signs are the same, add; if the signs are different, subtract and give the answer the sign of the largest number.

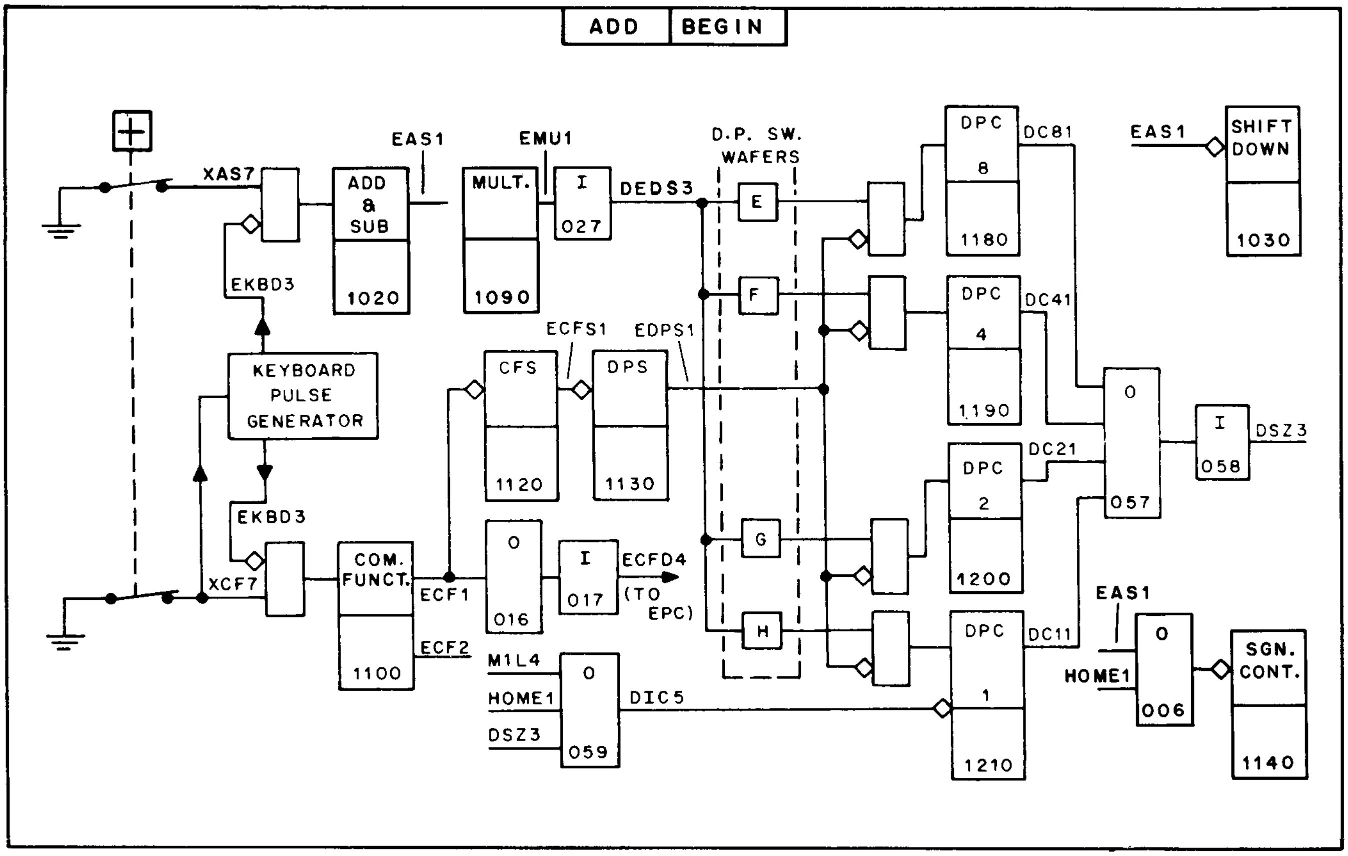
In the machine, in a machine add operation, the addition is done by counting data into the A Counter; holding that data setting in the A Counter while simultaneously transferring the data to the B Counter; then counting new data into the A Counter "on top of" the setting left by the previous data.

During the "add" count into A Counter, if the counter setting advances past 9 (representing 10 or more), a carry of 1 is placed into the next column add cycle. When all columns have been added in turn, the answer has been developed, and will be displayed in Register one.

OVERFLOW LOCK Key lights and the keyboard "locks up" if the last column (C14) addition develops a carry. The carry is a valid part of the answer and there is no further column in which to place the carry; therefore, machine capacity to display the answer has been exceeded.

ADD - BEGIN

SET FUNCTION FF's. Pressing ADD (+) Key on the keyboard closes Add reed switch and, by means of an interlocking code bar, also closes Common Function (CF) reed switch. Closing CF switch enables the Keyboard Pulse Generator, which produces the Keyboard Delay (EKBD3) pulse approximately 6 milliseconds later, and also enables an AC gate at the set input of CF FF. Closing Add reed switch also enables an AC gate at the input of ADD + SUB FF.



EKBD3 sets both CF and Add + Sub FF's. Setting of Add + Sub FF produces a +transition at set output (EAS1) which sets Shift Down FF. True output (EAS1) from set side of Add + Sub FF is also applied to O-006 at the set input of Sign Control FF, and ensures that SC is set.

SET DPC. At the same time, Multiply FF set output (EMU1), which will be False since function is Add and Mult. FF is reset, is inverted True by I-027, designated DEDS3, and applied through the Decimal Point (D.P.) switch wafers to enable AC gates on the set inputs of the Decimal Point Counter (DPC) FF's. Only those AC gates which have active connections through the switch wafers (see DPC discussion) will be enabled, and this, in turn, is controlled by the D.P. switch setting.

Meanwhile, closing of CF reed switch enabled an AC gate on CF set input. EKBD3 (True) transition sets CF. Setting of CF causes set output (ECF1) to transition False to True which sets Common Function Storage (CFS) if CFS is in a reset condition. CFS will be reset only if the last operation performed at the Keyboard was a number entry. If the number is not decimal aligned by ENTER Key, then the first step of any function is to Decimal Align. However, if the last operation at the Keyboard was a function, then the number in R1 is already decimal aligned and CFS is set, therefore CF set cannot set CFS and no setting is placed into the DPC. CFS set causes set output (ECFS1) to transition False to True which sets Decimal Point Storage (DPS). DPS set causes set output (EDPS1) to transition False to True and this transition is applied to AC gates at the set inputs of all DPC FF's. However, only the AC gates enabled by DEDS3 applied through the D.P. switch wafers are affected by the transition, and only those FF's are set. Thus DPC sets to a number that correlates with the decimal point position as chosen by the D.P. switch.

UNCLAMP EPC. ECF1 True is applied through O-016 to I-017, and inverted False, designated ECFD4. Previous to the set of CF, the CF set output (ECF1) was False, inverted True by I-017 (ECFD4), and, applied to diodes at the reset outputs of all EPC FF's, clamped EPC to 0. When ECFD4 goes False, this removes the clamping action of the diodes at EPC, and EPC is free to be stepped off zero (0).

Step of EPC, designated PIC5, is controlled by O-024. If all inputs are False and one goes True, the output of O-024 transitions False to True, and this transition applied to EPC1 FF T-input changes the state of EPC1, which advances EPC by 1. The next HOME1 at O-024 after ECFD4 goes False will step EPC to 1.

ADD - EPC1

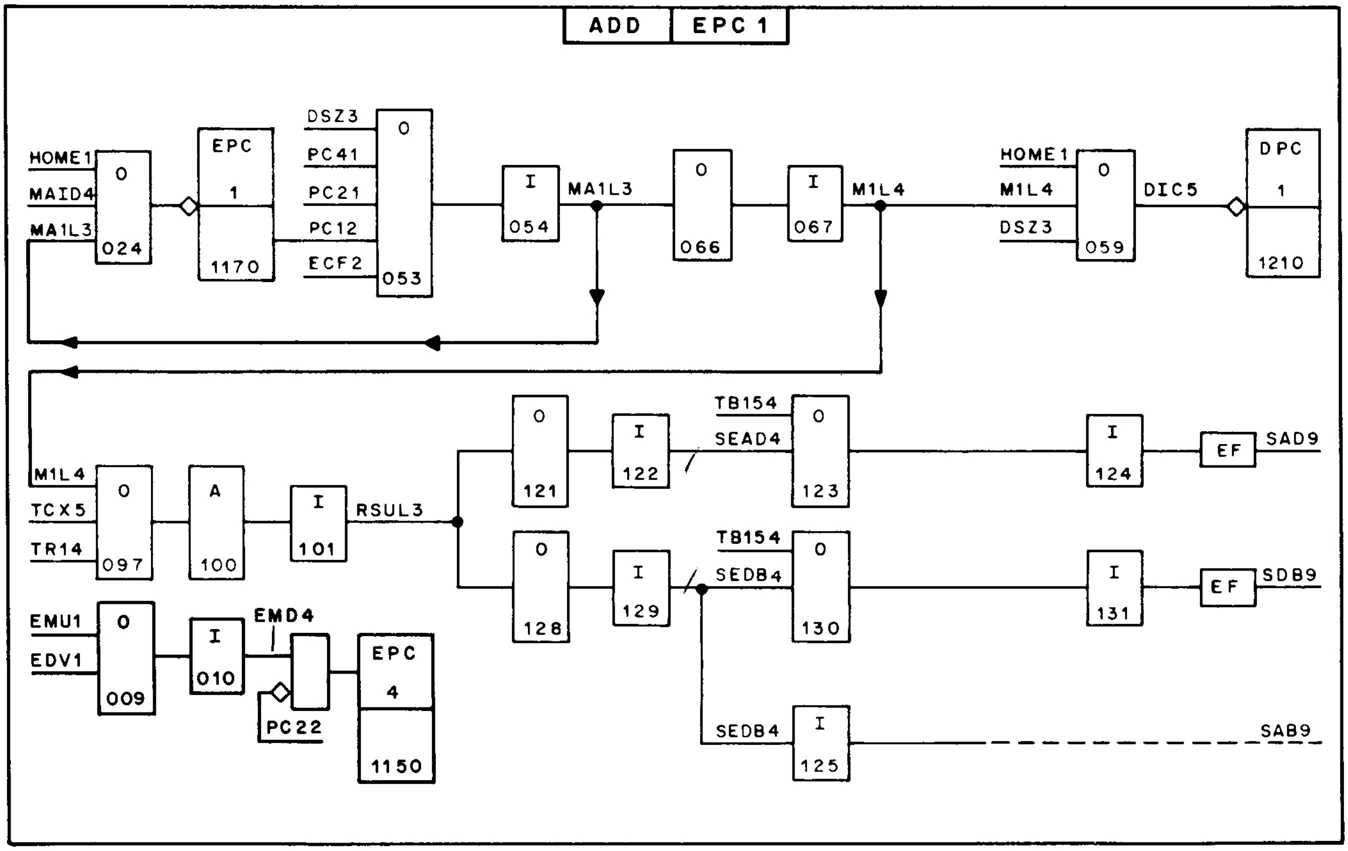
The logic action in EPC step 1 of Add function is to decimal align the number in Register one if the number has not already been aligned by ENTER Key. During BEGIN of Add function, DPC is set to the proper number for the decimal alignment if the last operation was a number entry. DPC FF settings specify the number of times that the digits in R1 will be shifted left in order to put the whole number portion of the total number of entered digits to the left of the decimal point on the display.

INHIBIT DISPLAY. When EPC steps off zero, PSZ3 (I-032) goes False. PSZ3 is applied at A-225 in the Display Timing to enable display when True. Therefore, on any EPC step other than zero, Display is inhibited because PSZ3 is False. Display will not be enabled until PSZ3 again goes True, which will be at the end of the function.

DECIMAL ALIGN. "Align Shift 1 left" (MA1L3) is developed by I-054 controlled by O-053 acting as a -AND. The logic inputs to O-053 specify DSZ3 False, ECF2 False, and EPC step 1 False (PC41, PC21, PC12). When all inputs to O-053 are False, the output is False and is inverted True by I-054, designated MA1L3. MA1L3 is applied to O-024 as an inhibit signal to keep EPC from stepping off 1 until all the shifts left are completed. MA1L3 is also applied through O-066 to I-067 and inverted False, designated M1L4. M1L4 enables O-059, which permits DPC to be counted up by one each HOME1 until DPC reaches zero (DSZ3 will be False until DPC reaches zero).

M1L4 is also applied to enable O-097. TCX5 is True for C0, C1, and C15 time, thus is False at O-097 for C2 through C14 time. TR14 goes False at R1 time. Thus, the output of O-097 is False for R1 time from C2 through C14 time as long as M1L4 is False. O-097 False is applied through A-100 to I-101 and inverted True, designated RSUL3 (enable shift up or left). RSUL3 is applied through O-121 to I-122, inverted False, designated SEAD4, and applied to enable O-123. TB154 specifies that the output will be False each B15 time as long as O-123 is enabled by SEAD4. False output of O-123, inverted True by I-124, is applied through an emitter-follower as SAD9 to shift A Counter data setting to D Counter (A to D), which is a part of Shift Left.

RSUL3 is also applied through O-128, inverted False by I-129, designated SEDB4, and applied to enable O-130. TB154 input to O-130 specifies that the output of O-130 will be False each B15 time as long as O-130 is enabled by SEDB4. False output of O-130, inverted True by I-131, is applied through an emitter-follower as SDB9 to the counter



circuits to Shift D Counter data setting to B Counter (D to B), which is a part of Shift Left.

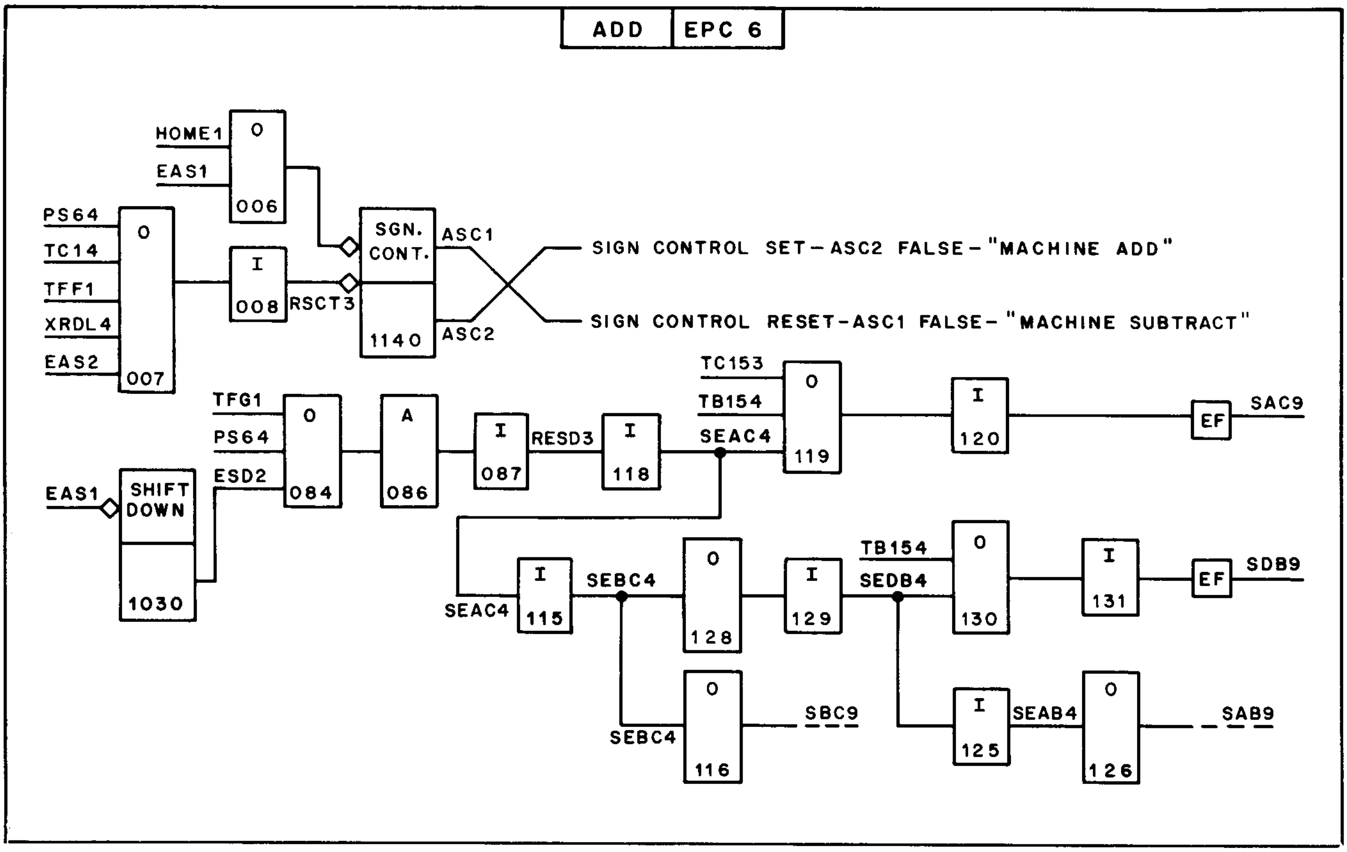
SEDB4 is also inverted True by I-125 and applied to inhibit O-126, which inhibits A to B Shift. This is so that A to B and D to B shifts cannot occur together. Two simultaneous inputs to the same counter is never desired, thus, when D to B is called for, A to B is inhibited.

ADD - EPC6

STEP EPC TO 6. At the end of EPC1, Home1 would normally step EPC to 2. This is not desired in Add function. Instead, EPC steps from 1 to 6, which is specified by I-010 (EMD4) controlled by O-009. When both Mult and Divide FF's are reset, which they will be in Add, the output of O-009 is False, and, inverted True by I-010, designated EMD4, enables an AC gate at set input of EPC4 FF. Normal stepping of EPC1 to EPC2 is from EPC1 set, EPC2 reset, EPC4 reset to EPC1 reset, EPC2 set, EPC4 reset. However, when EPC2 sets, EPC2 set output (PC21) goes True and is applied as a + transition to the AC gate enabled by EMD4 at the set input of EPC4, and EPC4 sets. Thus, EPC ends up with EPC1 reset, EPC2 set, EPC4 set, which is specified as EPC step 6.

COMPARE SIGNS. In EPC6 the logic derives a decision that will place the actual machine performance into "machine add" or "machine subtract". In ADD-BEGIN, HOME1 True through 006 sets SC. When Add-Subtract FF sets, EAS1 goes True and is applied at O-006 to inhibit any further action by HOME1 True on SC FF. At the same time, EAS1 True insures that SC FF is set in order that the start of "Compare signs" is with SC set in an Add function. O-007 at the Sign Control FF T-input is enabled at EPC6 (PS64), and during C1 time (TC14), Add or Subtract function (EAS2), TFF1 (R1 and R2 time), the output pulses of the Read amplifier (XRDL4), which are the data pulses in C1R1 and C1R2 time (if any), will cause the output of O-007 to go False. False output of O-007, inverted True by I-008, designated RSCT3, is applied to the T-input of Sign Control FF.

If both signs (R1 and R2) are +, there are no data pulses in C1R1 and C1R2 time, therefore SC remains set and function is "machine add" because signs are the same. If both signs (R1 and R2) are -, there is one pulse in C1R1 time and one pulse in C1R2 time. C1R1 pulse, through O-007 and I-008, resets SC FF, and C1R2 pulse, through O-007 and I-008, sets SC FF again, therefore SC ends up set and function is "machine add" because signs are the same. If signs are different there will be only one data pulse (- sign), which can be in either C1R1 or C1R2, and SC FF then ends up reset and function is "machine subtract".



SHIFT DOWN. To perform a computation, data in R1 is shifted down to R0, which is an undisplayed register, and R2, R3, and R4 are also shifted down one register. This is controlled by O-084. Logic inputs to O-084 specify Shift Down FF set (ESD2), EPC step 6 (PS64), TFG1 (R1 through R4) and the output will be False for R1 through R4 time in an Add function EPC step 6. False output of O-084 is applied through A-086 to I-087 and inverted True, designated RESD3. RESD3 applied to I-118 is inverted False, designated SEAC4. SEAC4 is applied to enable O-119. Logic inputs to O-119 specify a False output each B15 time for all C times except C15 (C15 is used only in a Divide function). False output of O-119, inverted True by I-120, is applied through an emitter-follower as SAC9 to initiate shifts of data from A Counter to C Counter each B15 time from C1 through C14 time as long as O-119 is enabled by SEAC4.

SEAC4 is inverted True by I-115, designated SEBC4. SEBC4, when True, inhibits O-116, which inhibits B to C shift when A to C is designated. SEBC4 is also applied through O-128 to I-129, inverted False, designated SEDB4 and applied to enable O-130. TB154 at O-130 specifies a False output from O-130 each B15 time as long as SEDB4 is False. O-130 False output, inverted True by I-131, is applied through an emitter-follower as SDB9 to initiate shifts of data from D Counter to B Counter. This D to B shift is pertinent primarily to R4 data, and is used to put zeroes in R4 time when R4 data is shifted to R3. SEDB4, inverted True by I-125, designated SEAB4, is applied to inhibit O-126, which inhibits A to B shift when D to B shift is designated.

Shift Down (A to C, D to B) takes one pass of data through the counters. The next HOME1 at O-024 steps EPC to 7.

ADD - EPC7

In EPC step 7, R1 data is added to R0 data in A Counter. This is accomplished by counting R0 data into A Counter, then inhibiting reset of A after the A to B shift. This leaves R0 data in A Counter. R1 data is then counted into A "on top" of R0 data, which effectively adds R1 to R0.

COUNT R0 IN A. Count in A (CIA9), which is the same for both R0 and R1, is initiated by I-152. Data pulses (False) from the Read Amplifier (XRDL4) are inverted True by I-152, designated MAIR3. MAIR3 pulses are applied through O-153 to I-154 and inverted False. False output pulses of I-154 are inverted True by I-155 and applied through an emitter-follower as CIA9 to A Counter. A Counter, then, attains a setting that corresponds to the number of data pulses in a given R time.

INHIBIT RESET A. Inhibit of reset A, which is developed at R0 time, is controlled by O-074. The enable on O-074, which is MAD4, is controlled by O-021. The inputs to O-021 specify Add or Subtract function (EAS2), SC set (ASC2), and EPC step 7 (PS74). False output of O-021 inverted True by I-022, designated MAIS3, is applied through O-018 to A-019. If COF is not set, ACOF2 is True, and MAIS3 and ACOF2 will make A-019 output True. True output of A-019, inverted False by I-020, designated MAD4, enables O-074. TCX5 on O-074 specifies C2 through C14 time, and TR04 specifies R0 time. The output of O-074 will be False during R0 time from C2 through C14 time as long as O-074 is enabled by MAD4 being False. False output of O-074, inverted True by I-075, designated AIRA3, is applied to O-140 and inhibits the development of CRA9 (True) which would otherwise occur at R0B15 time. For CRA9 to be True, which is reset A, both inputs to O-140 must be False. However, AIRA3 is True and makes CRA9 False, which cannot reset A, thus inhibit (block) reset A.

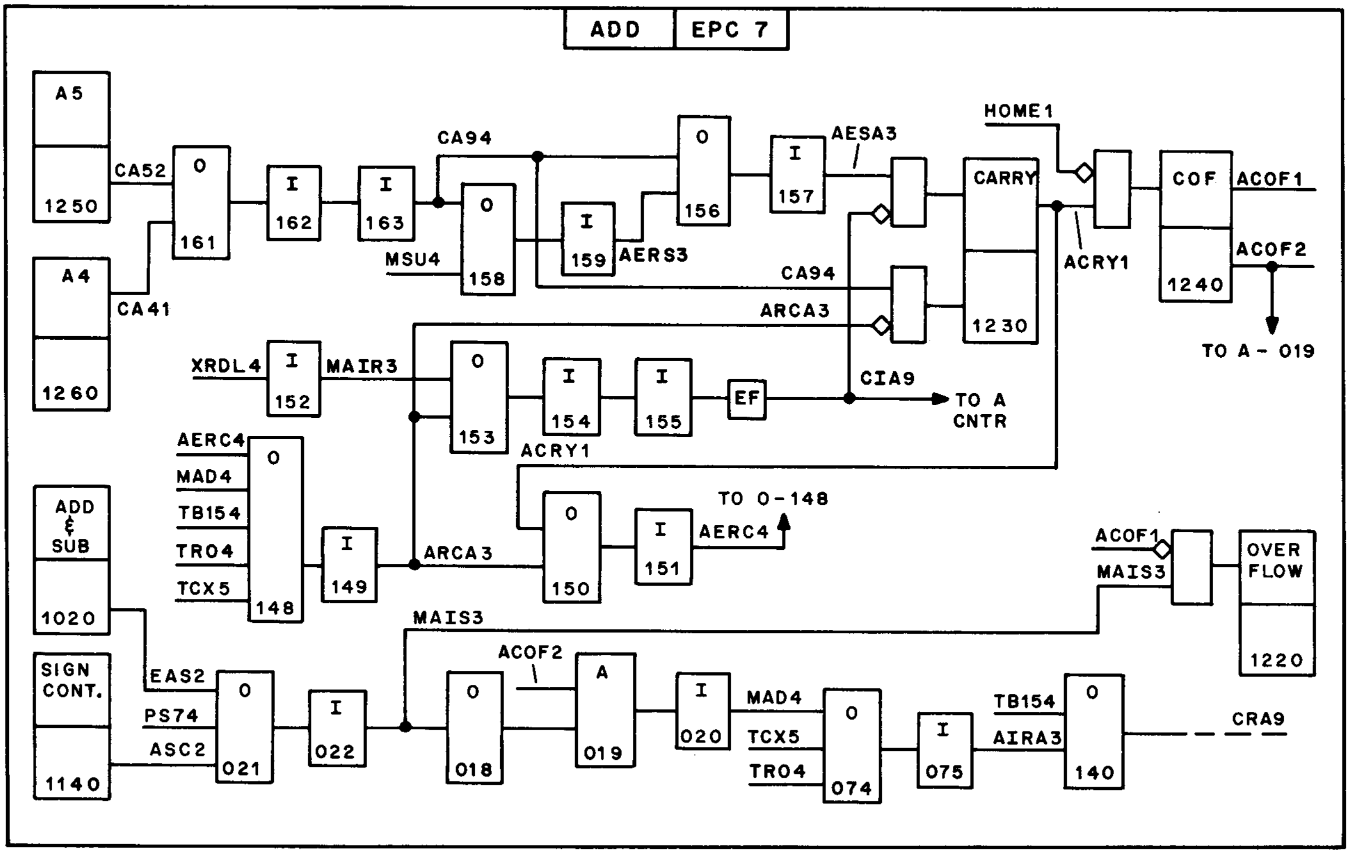
IS CARRY SET? Later in the add cycle of the Flow Chart in EPC step 7, the Add R0 to R1 may count A past 9. The first time through cannot find Carry set because no add has yet taken place in the Flow Chart. However, any add cycle may make Carry set, and if Carry is set, 1 is added to A to show the Carry.

ADD 1 TO A. When A counts past 9, which can occur during "add R0 to R1", and sets Carry, this indicates an "add 1 to A" for the next column add cycle. This is controlled by O-148. Inputs to O-148 specify R0 time (TR04), Add function (MAD4), C2 through C14 time (TCX5), and B15 time (TB154). AERC4 input to O-148 is controlled by O-150.

If Carry is set at Home time, Carry Overflow sets and ACRY1 is True, and applied through O-150 to I-151 is inverted False, designated AERC4. AERC4, then, enables a False output from O-148 when all other inputs are False, which will be at R0B15 time for C2 through C14 time when Carry is set during an Add function. Since Carry cannot set until R1 data counts A past 9, the next R0 time is in the next column time, and that is when the 1 will be added to A.

The add 1 to A signal is ARCA3 (True) applied to develop CIA9 through O-153, the output of which is doubled inverted by I-154 and I-155. The ARCA3 pulse acts exactly as a pulse from the Read amplifier to count A up by one, except that ARCA3 occurs just before R1 time (R0B15) when no Read pulses are present from the delay line.

RESET CARRY. Set of Carry was enabled when CA94 was False at O-156. The same CIA9 pulse that set Carry also counted A past 9, which makes CA94 True. CA94 (True) is applied to enable an AC gate (1235) on Carry reset input. The same ARCA3 pulse that Adds 1 to A resets Carry.



SPECIAL CASE. There is a possibility, however, that the pulse that adds 1 to A finds A Counter already at 9, which would make A count past 9 indicating a further carry. Yet ARCA3, which adds 1 to A, attempts to reset Carry. CA94 will be False at any time A Counter is 9 and, at AC reset gate 1235, will inhibit reset of Carry if the Add 1 to A finds A at 9. Thus Carry remains set to indicate this further carry in the next column add cycle.

ADD R0 TO R1. Add R0 to R1 is accomplished by simply counting R1 into A Counter on top of R0 data setting left in A by the inhibit of reset A.

DID A COUNT PAST 9? CA94 at O-156 is controlled by O-161. When A Counter is 9, A4 is reset and A5 is set. CA41 and CA52 at O-161 are False, O-161 output is False, and double inverted by I-162 and I-163, designated CA94, will be False at O-156.

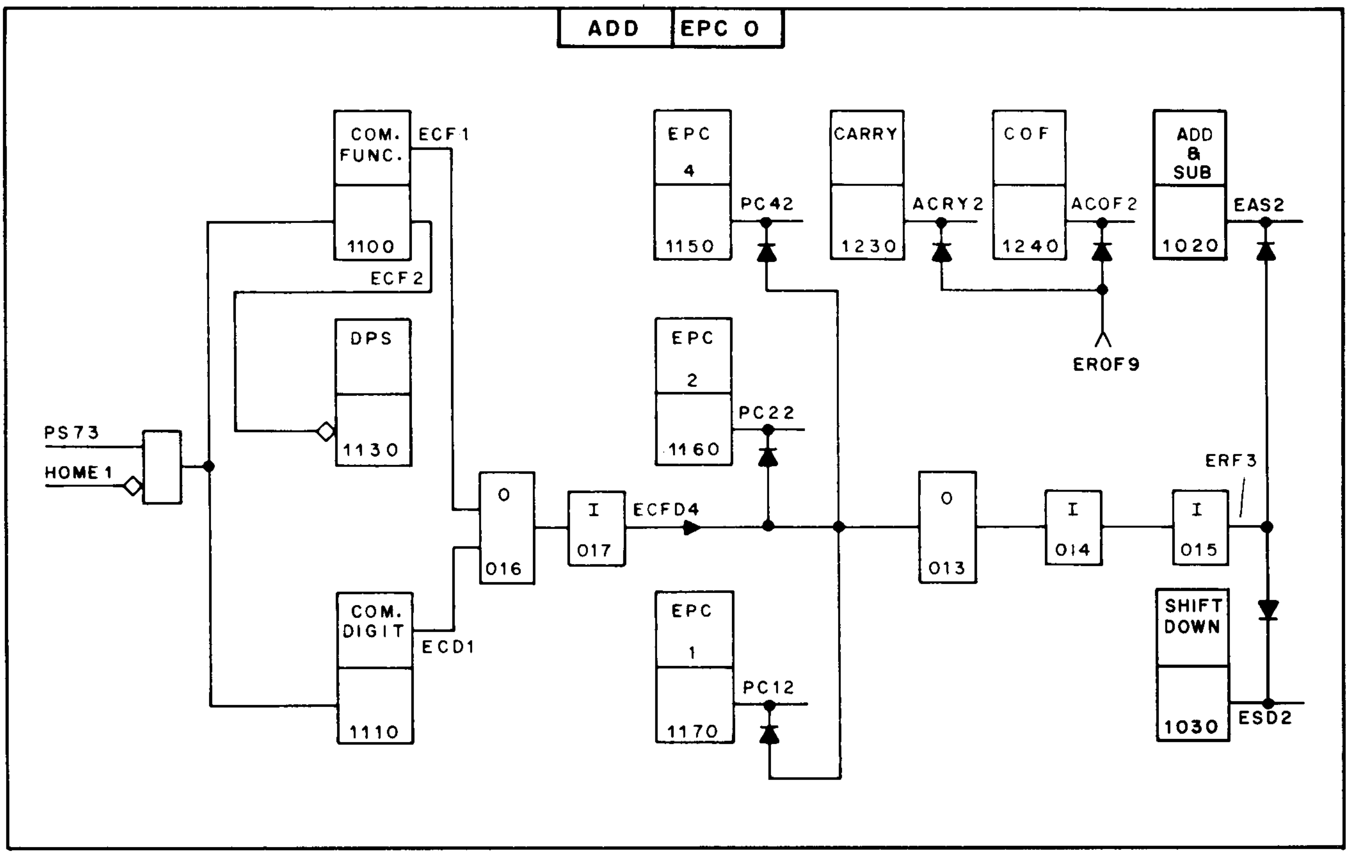
SET CARRY. Carry FF set is initiated by an AC gate (1232) on set input, which is enabled by AESA3. AESA3 is initiated by MSU4 on O-158. MSU4 will be True since function is Add and MSU4 is False only during Subtract. True output of O-158 is inverted False by I-159, designated AERS3. AERS3 is one input to O-156. The other input is CA94, which will be false when A Counter is 9. False output of O-156, inverted True by I-157, designated AESA3, enables the Carry FF set input AC gate. The next CIA9 pulse, which also counts A to 10, sets Carry FF. When A is at 10 (0), or any number other than 9, CA94 is True and AESA3, then, is False and inhibits the AC gate on Carry FF. Therefore Carry can be set only by the CIA9 pulse that counts A past 9. Carry being set at the next column add cycle will add 1 to A, as has been explained previously in the Flow Chart.

IS COF SET BY HOME? If C14 add cycle leaves Carry set, ARCA3 cannot reset Carry because TCX5 True on O-148 inhibits the gate after C14 time, thus ARCA3 will be False in C15 time. Therefore, HOME1 finds Carry set, and sets COF through O-160 output at AC gate 1241 on COF FF set input.

SET OVERFLOW FF. ACOF1 (True) is applied to an AC gate at Overflow FF which is enabled by MAIS3 being True, and sets Overflow FF. Overflow FF set designates an overflow condition which lights OVERFLOW LOCK key and sets keyboard interlock. The same HOME1 that sets COF, thus Overflow FF, at the same time steps EPC to zero (0).

ADD - EPC0

CLAMP EPC. PS73 (True) is developed at



EPC step 7 by O-033 output (False) inverted True by I-034, and is applied to enable an AC gate which is common to the reset inputs of CF and CD. The same HOME1 that steps EPC to 0, resets CF or CD, whichever is set, in this case, CF. CF reset transition resets DPS. ECD1 and ECF1 at O-016 are both False with CF and CD reset, and False output of O-016 is inverted True by I-017, designated ECFD4. ECFD4 (True) is applied to diodes at EPC FF reset outputs, and clamps EPC to zero (0).

RESET FUNCTION FF's. ECFD4 is also applied through O-013 to I-014, and double inverted by I-014 and I-015, designated ERF3. ERF3 (True) is applied to reset outputs of all function FF's and resets any that are set.

ENABLE DISPLAY. When EPC is at zero, PSZ3 is True and is applied in the Display timing circuitry to permit Display. Add function is completed.

2. SUBTRACT FUNCTION

As in the Add function, there is a distinction between a Subtract function chosen by pressing the Subtract (-) key on the keyboard and an internal "machine subtract". Machine decision to subtract is made on the basis of the algebraic signs.

The algebraic rules are: If the signs of the numbers are the same, subtract. If the signs of the numbers are different, add and give the answer the sign of the number in R2.

In the machine, in a machine subtract operation, the subtraction is done by "complementary addition". One method of subtraction is to subtract one number from another by adding the complement of one of the numbers to the other number. The complement of a one-digit number is the difference between that number and ten; the complement of a two-digit number is the difference between that number and 100; the complement of a three-digit number is the difference between that number and 1000, etc.

The basic machine operation in a machine subtract is done by counting R0 into D Counter; shifting D Counter setting, which is the complement of R0, to A Counter; then counting R1 into A Counter "on top of" the D Counter setting. Counting R0 into D Counter initiates a borrow, and, if the count in A advances past 9, the borrow is cancelled. If the borrow is not cancelled, the next count in D will start from 9, thus giving the 9's complement. The borrow will not be cancelled until an "Add in A" results in a carry.

If the borrow is not cancelled when the last column (C14) is added, the machine complements the answer and changes the sign. For example, when subtracting a larger number from a smaller number, such as 12 from 6, by machine subtract (complementary add) the answer would be 94, which is obviously wrong. However, if the developed answer (94) is again complemented it becomes 06, and is a correct answer. The second complement, in this case, develops a negative sign that is displayed to show that it is a negative number. The machine recognizes the fact that the answer must be complemented and displayed with a changed sign by the presence of a borrow (COF set) when all columns have been subtracted.

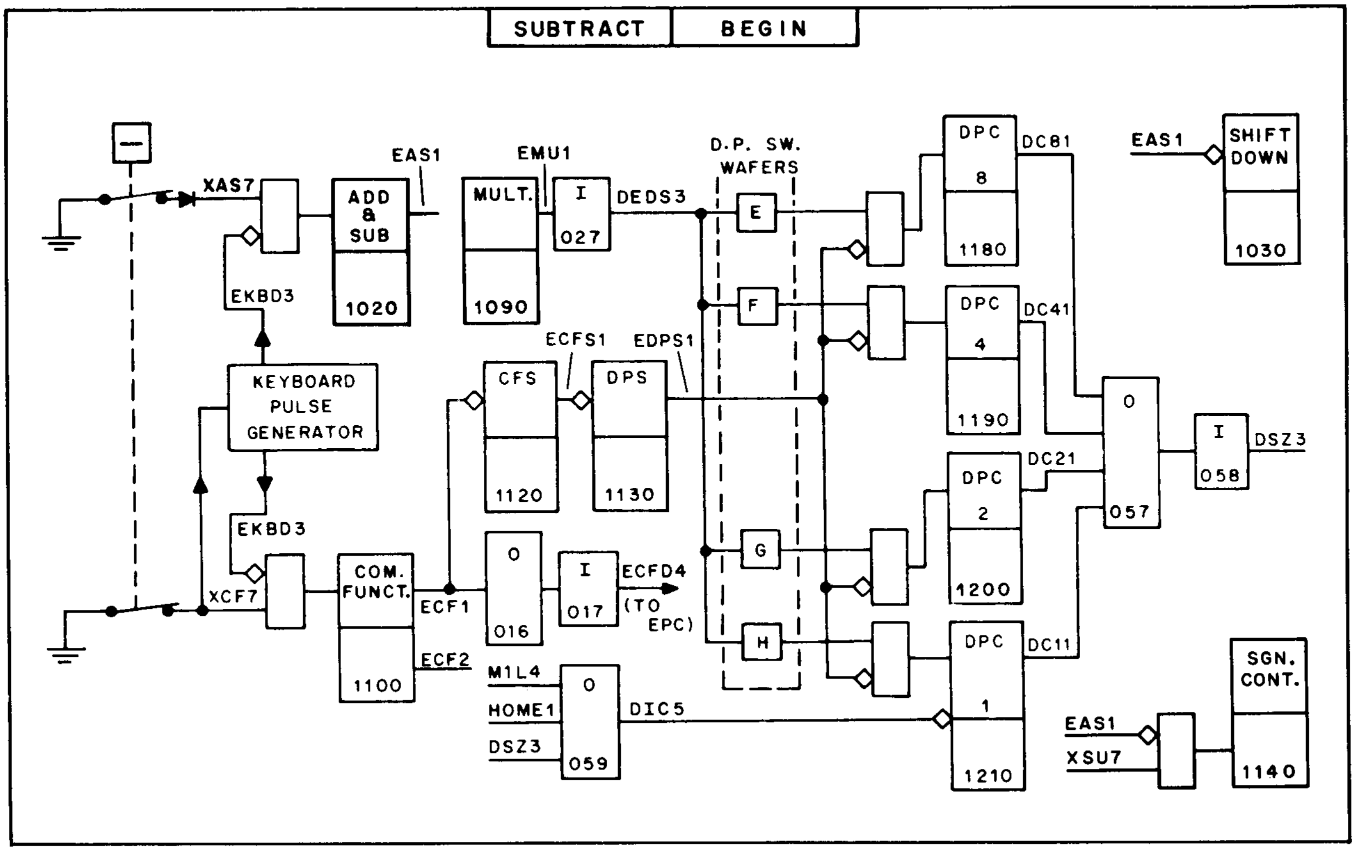
SUB-BEGIN

SET FUNCTION FF's. In Add function pressing Add Key initiated action which ended with A + S FF set. In Subtract, the A +S FF becomes set by pressing Subtract (-) Key which, through an isolation diode, enables an AC gate at the set input of A +S FF. Also, as in Add, pressing Subtract Key closes CF reed switch through an interlocking code bar, which enables an AC gate on CF FF set input and also initiates keyboard delay (KBD). Approximately 6 milliseconds later A + S FF and CF FF become set by the KBD +transition (EKBD3). CF set output (ECF1) False to True transition sets CFS, which, in turn, sets DPS if CFS is in a reset condition. CFS will be reset only if the last operation performed at the keyboard was a number entry. If the number is not decimal aligned by ENTER Key, then the first step of any function is to Decimal Align. However, if the last operation at the keyboard was a function, then the number in R1 is already decimal aligned and CFS is set, therefore CF set cannot set CFS and no setting is placed into DPC.

SET DPC. DPS set output (EDPS1) False to True transition sets those DPC FF's which have been enabled through the D.P. switch wafers and DPC becomes set for decimal alignment exactly as in Add function (See Add - Begin).

RESET SIGN CONTROL FF. In Add function, SC FF is set by Home at O-006 and remains set unless signs of R1 and R2 are unlike. In Subtract, closing Subtract reed switch enables an AC gate at the reset input of SC FF. Now, when A + S FF sets, the False to True transition (EAS1) at the AC gate resets SC FF, which is the requirement for a "machine subtract" operation.

SET SHIFT DOWN FF. "Set" of A + S FF produces a False to True transition at A+S set output (EAS1) which is applied to set input of Shift Down FF, and sets Shift Down.

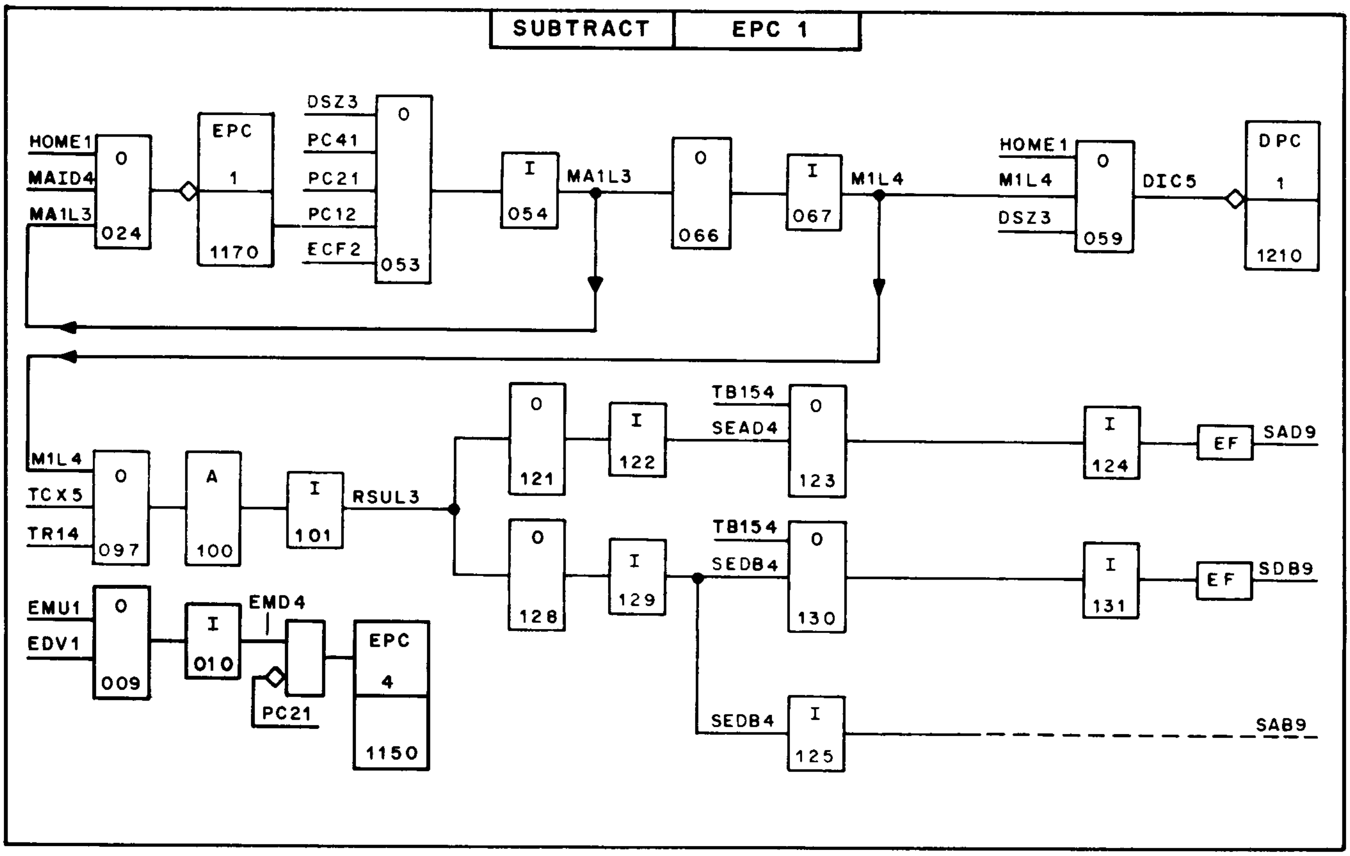


SUB - EPC1

INHIBIT DISPLAY. When EPC steps off zero, PSZ3 (I-032) goes False. PSZ3 is applied at A-225 in the Display Timing to enable display when True. Therefore, on any EPC step other than zero, Display is inhibited because PSZ3 is False. Display will not be enabled until PSZ3 again goes True, which will be at the end of the function.

DECIMAL ALIGN. At EPC step 1 in subtract, the number in R1 is shifted left the requisite number of times that will place the whole number portion to the left of the decimal point if the number has not already been aligned by the ENTER key. The number of shifts left, in turn, is controlled by the DPC setting that was established at Begin condition, and this, in turn, is controlled by the specific Decimal Point switch setting. The "Shift Left" action is exactly as described for Add function, EPC step 1.

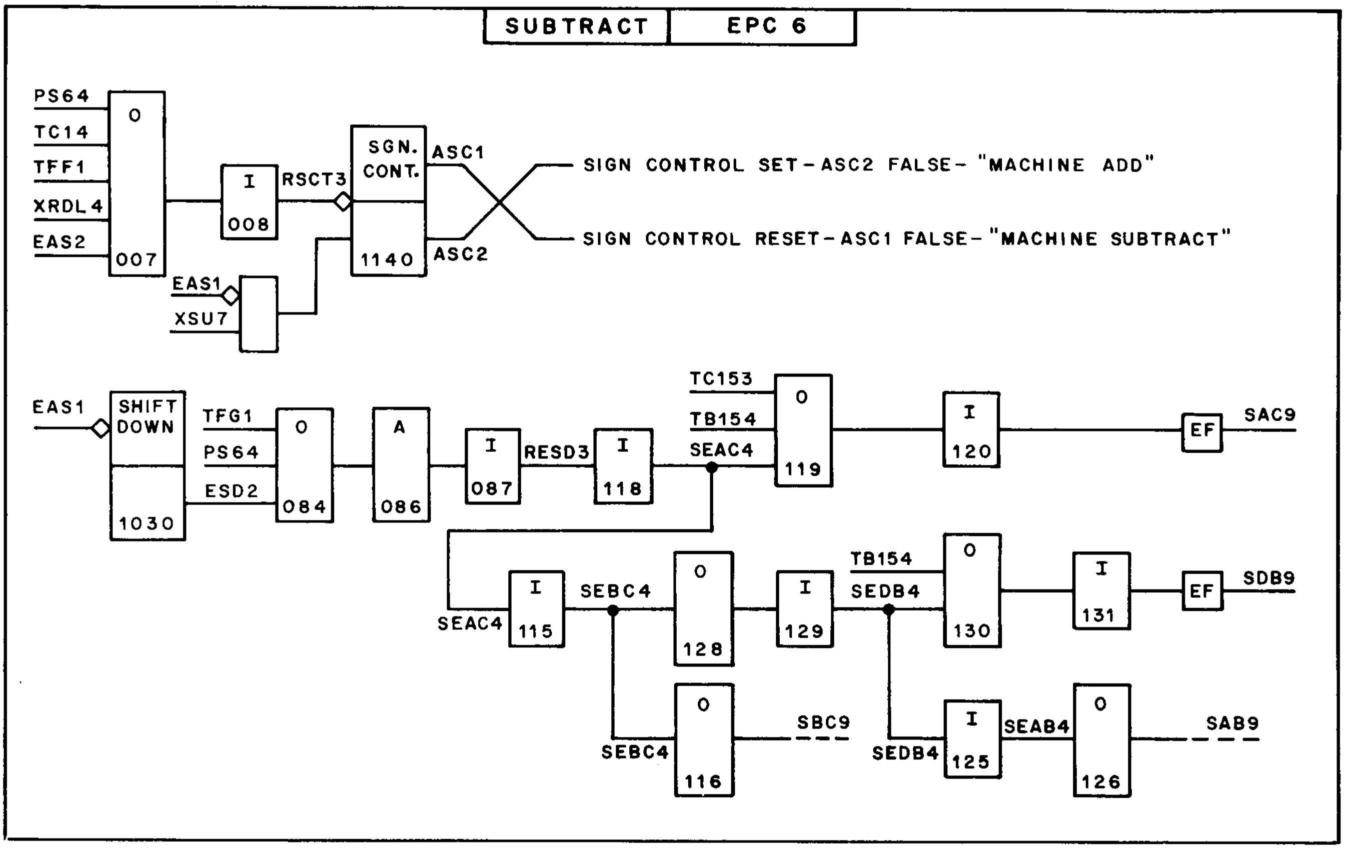
STEP EPC TO 6. As in Add function, EPC steps from 1 to 6 instead of from 1 to 2, in exactly the same manner and with the same logic control gates.



SUB - EPC6

COMPARE SIGNS. An important step in EPC6 is to compare the signs of R1 and R2 and this is done in exactly the same manner as in Add function. However, in Subtract function, SC FF starts from reset condition. Thus, if signs of R1 and R2 are the same, SC FF ends up reset and "machine subtract" takes place. If signs are not the same, there will be only one sign pulse present in either C1R1 or C1R2 and SC FF ends up set, thus "machine add" takes place and logic action is as specified under Add Flow Chart (EPC6).

SHIFT DOWN. Also, in EPC6, registers R1 through R4 shift down exactly as in Add function, which places R1 into R0 for computational purposes, and, when Shift Down is complete, Home steps EPC to 7.



SUB - EPC7

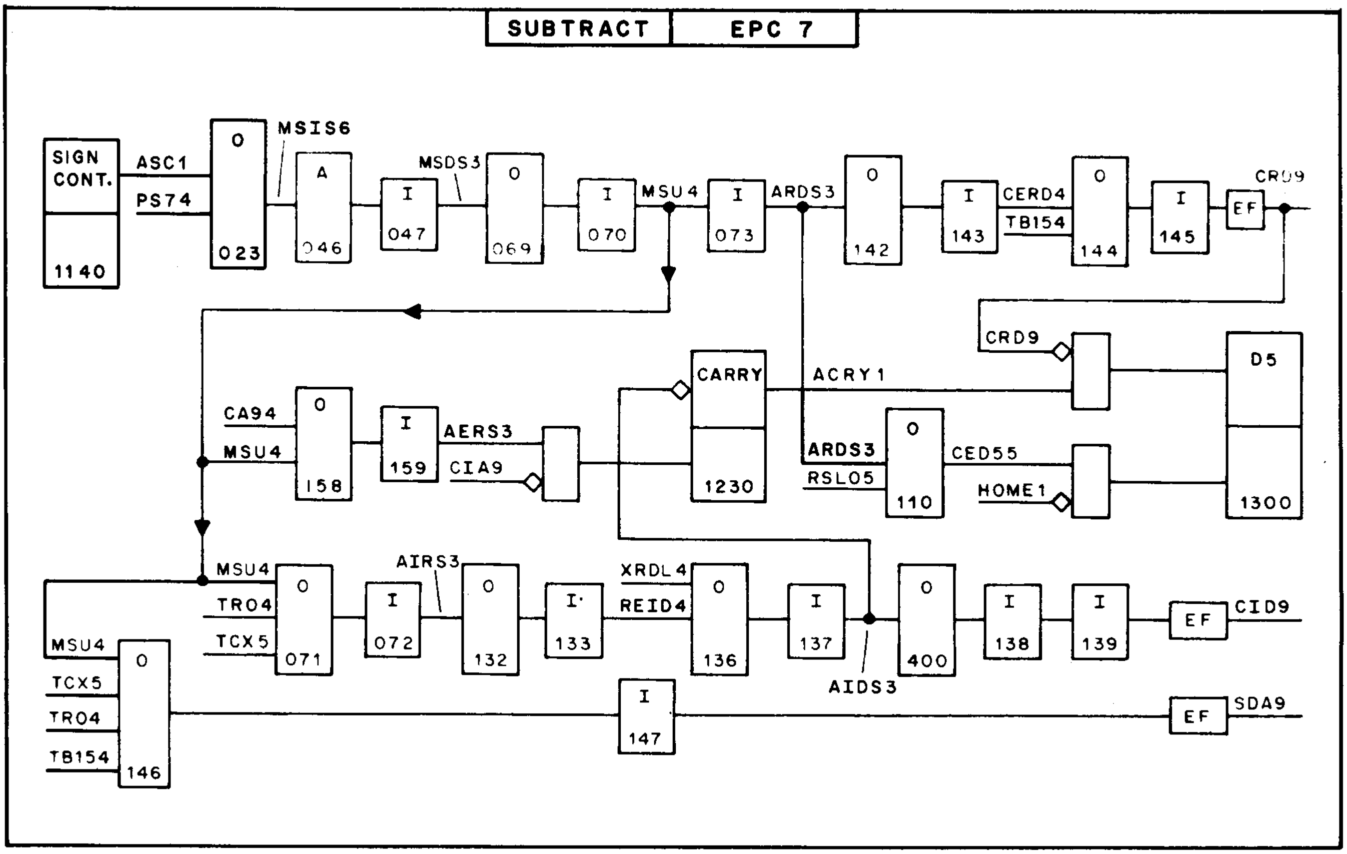
Since Subtraction is done by complementary addition, R0 data must be complemented and added to R1. Complementation is done by "Count in D". D Counter is a "down" counter, thus, counting the data pulses from the line into D produces the complement of the number represented by the data pulses. Data pulses are counted into A Counter and D Counter simultaneously. The "count in A" preserves R0 data in the data sequence via a normal A to B shift at the end of R0 time (R0B15).

COUNT R0 IN D. When SC FF is reset, ASC1 is False and enables O-023. The other input to O-023 specifies EPC7, and the output (MSIS6) will be False if SC is in reset during EPC step 7. MSIS6 is applied through A-046 to I-047 and inverted True, designated MSDS3. MSDS3 is applied through O-069 to I-070 and inverted False, designated MSU4, which is applied to enable O-071. The other logic inputs to O-071 specify R0 time (TR04) and C2 through C14 time (TCX5). Thus, the output of O-071 will be False during R0 time from C2 through C14 time as long as MSU4 is False. False output of O-071, inverted True by I-072, designated AIRS3, is applied through O-132, inverted False by I-133, designated REID4 and applied to enable O-136. The other input to O-136 is negative pulses from the Read amplifier (XRDL4), thus the output of O-136 will go False with each Read pulse as long as REID4 is False. False output pulses of O-136 are inverted True by I-137, designated AIDS3. AIDS3 True pulses are applied through O-400 to I-138 and double inverted by I-138 and I-139, end up True and are applied as CID9 to advance D Counter (Count in D).

SET CARRY. The first AIDS3 (True) is applied to set input 1231 of Carry FF, and sets Carry.

SHIFT D TO A. At the end of R0 time, the setting of D Counter, which indicates the complement of R0 data, is shifted D to A. This is controlled by O-146, enabled by MSU4. MSU4 indicates Subtract function. The other logic inputs to O-146 specify C2 through C14 time (TCX5), R0 time (TR04), and B15 time (TB154). The output of O-146 will go False each R0B15 during a subtract function from C2 through C14 time. O-146 False output, inverted True by I-147, is applied through an emitter-follower as SDA9 to the counter circuits to initiate a D to A shift each R0B15 time.

INHIBIT RESET A. "Reset A" (CRA9) would also occur at this time (R0B15) if not inhibited. In order that no conflict occur, in that R0 data might be shifted into A and reset out, the True output of I-072 (AIRS3) is applied to O-140, which inhibits "reset A" by making CRA9 False.



ADD R0 TO R1. Immediately after the D TO A shift, which put D Counter data (complemented R0 data) into A Counter, CIA9 pulses start counting A Counter up from the R0 setting, effectively adding R1 to R0. XRDL4 pulses inverted True by I-152, designated MAIR3, are applied through O-153 to I-154, double inverted by I-154 and I-155, and applied through an emitter-follower as CIA9 to advance A Counter (Count in A).

DID "A" COUNT PAST 9? When R1 is counted into A "on top" of R0 for the add cycle, if R1 counts past 9 it would indicate a carry, as in a normal add. This carry cancels the borrow. This is controlled by O-161 whose inputs are set output of A4 (CA41) and reset output of A5 (CA52). When both these inputs are False, A Counter setting indicates 9, O-161 output is False, and double inverted by I-162 and I-163, designated CA94, enables O-158.

RESET CARRY. The other input to O-158, MSU4, indicates Subtract function and the output of O-158 will be False, inverted True by I-159, designated AERS3 and enables an AC gate (1234) at reset input of Carry FF. The next CIA9 pulse, which would count A to 10, also resets Carry FF, which effectively cancels the borrow that was indicated by Carry being set by AIDS3.

IS CARRY SET? If the add R0 to R1 add cycle does not count A past 9, Carry FF, which was set by AIDS3 at the beginning of "Count in D", remains set. This indicates that the borrow was not cancelled and the next "Count in D" must start from a D Counter setting of 9, which means taking the 9's complement of R0.

ADD 1 TO D. To take 9's complement D Counter must start from a setting of 9 which is accomplished by effectively counting 1 in D by inhibiting reset of D5 when all other D FF's become reset in preparation for the next "Count in D". ACRY1 is True when Carry is set and is applied to an AC gate at set input of D5 counter FF. Normally, at shift time (B15), D Counter is reset to zero in preparation for the next "Count in D". However, if the D5 AC gate is enabled by ACRY1 (True), D Counter is reset to 9 instead of 0 (10) which means the next "Count in D" starts from 9 instead of 0 (10), thus 9's complement is taken, which shows the presence of a borrow for the previous column.

The "complementary add" cycle takes place for all columns, C2 through C14, and, when all columns have been through the cycle, HOME1 at O-024 steps EPC to 0 and the arithmetic of the problem is complete.

SUB - EPC0

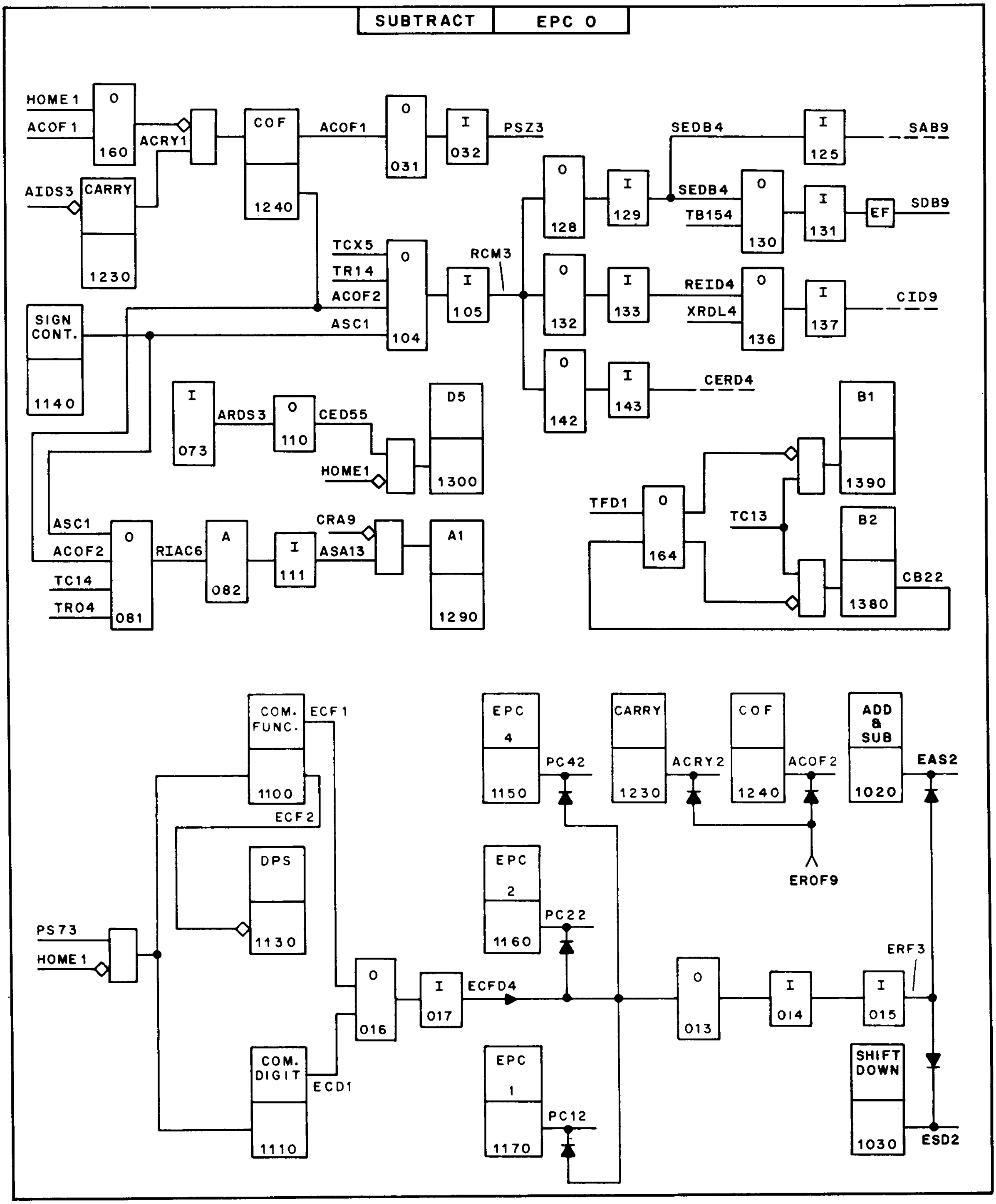
PS73 and HOME1 being True reset CF FF at the end of EPC7. CF reset enables ERF3 to go True at the output of I-015, which resets A + S FF, as well as any other function FF's that are set. A + S FF set output (EAS1) inhibited O-006 when True at set input of SC FF. The other input to O-006 is HOME1. It would appear, then, that immediately A + S reset, the inhibit on O-006 would be removed because EAS1 goes False. However, there is a short time after HOME1 before A + S actually resets and removes the inhibit, therefore, the same HOME1 that steps EPC to 0 cannot set SC FF, but the next HOME1 will. Thus, there is one word time after EPC0 before SC FF sets, and during this time R1 data is complemented and replaced in R1 time for answer display.

In Add, if Carry was set at Home time, an overflow condition was indicated. In subtract, Carry being set at Home time indicates that the answer in R1 is to be complemented before display, and the sign of the answer changed.

IS COF SET BY HOME? Carry being set at Home enables an AC gate on set input of Carry Overflow (COF). HOME1 sets COF through O-160, and ACOF2 goes False. At this time SC is reset because SC FF was placed reset in SUB-BEGIN when A + S FF became set, and ASC1 is False. ACOF2 and ASC1 are both False at O-104 and enable the gate. At R1 time (TR14), C2 through C14 time (TCX5), the output of O-104 will be False and inverted True by I-105, designated RCM3 (Complement). RCM3 is applied through O-132 to I-133, inverted False (REID4), and applied to enable O-136, which enables "Count in D" exactly as in SUB - EPC7. Count in D complements the data in R1, which is the answer data.

RCM3, applied through O-142 to I-143 and inverted False, designated CERD4, enables O-144 which develops reset D (CRD9) each B15 time as in SUB - EPC7.

ARDS3 developed by I-073 is applied at O-110. The last "Count in D" for C14 time would leave Carry set indicating a borrow, which would "add 1 to D" by setting D5. Leaving D5 set at this time is undesired because this is data in D, so ARDS3 (True) is applied through O-110 (CED55) to enable an AC gate at the reset input of D5, which allows Home to ensure that D5 is reset, and leaves D Counter set to zero.


SUBTRACT
EPC 0
HOME 1
ACOF 1
O
160
ACRY1
AIDS3
CARRY
1230
COF
1240
ACOF1
O
031
I
032
PSZ3
SEDB4
I
125
SAB9
O
128
I
129
SEDB4
TB154
O
130
I
131
EF
SDB9
TCX5
TR14
ACOF2
ASC1
O
104
RCM3
I
105
O
132
I
133
REID4
XRDL4
O
136
I
137
CID9
SIGN CONT.
1140
O
142
I
143
CERD4
I
073
ARDS3
O
110
CED55
HOME1
D5
1300
B1
1390
TFD1
O
164
TC13
B2
1380
CB22
ASC1
ACOF2
TC14
TR04
O
081
RIAC6
A
082
I
111
CRA9
ASA13
A1
1290
COM. FUNC.
1100
ECF 1
ECF 2
DPS
1130
EPC 4
1150
PC42
CARRY
1230
ACRY2
COF
1240
ACOF2
ADD & SUB
1020
EAS2
EROF9
EPC 2
1160
PC22
PS73
HOME 1
O
016
I
017
ECFD4
O
013
I
014
I
015
ERF3
COM. DIGIT
1110
ECD1
EPC 1
1170
PC12
SHIFT DOWN
1030
ESD2

SHIFT D TO B. RCM3 True is applied through O-128 to I-129, inverted False, designated SEDB4 and applied to enable O-130. When TB154 goes False at B15 time, the output of O-130 goes False and, inverted True by I-131, is applied through an emitter-follower as SDB9 to the counter circuits to initiate a D to B shift. Since RCM3 is limited to R1 time, the D to B shift occurs at the end of R1 time (R1B15). To prevent A to B shift at this time, SEDB4 False is inverted True by I-125 and inhibits O-126, thus no A to B shift.

CHANGE SIGN OF R1. One further step is to change the sign of R1. Assume R1 was +, there would be no sign pulse in C1R1B3 time. ASC1 and ACOF2 enable O-081. TC14 and TR04 inputs specify that at C1R0 time, the output of O-081, designated RIAC6, will be False and, applied through A-082 to I-111, will be inverted True, designated ASA13, ASA13 is applied to enable an AC gate at set input of A1 FF. When A Counter FF's are reset by CRA9 at the end of C1R0 time, A1 becomes set, thus 1 is added to A just before C1R1 time. Now, when C1R1 counts in A it will count "on top" of this 1 that was added. Since R1 was assumed to be +, there is no sign pulse in C1R1 time, and A remains at 1. At the end of C1R1 time, R1 is shifted to B, then to C, and on to the line. However, C1R1 now has a sign pulse in B3 time, thus a negative sign will be displayed and the sign of R1 has been changed.

Assume now that R1 is negative. This means a sign pulse in C1R1 time. This pulse added to the 1 which was added to A to C1R0 time means a count of 2 in A. At the end of C1R1 time this 2 is shifted to B Counter and B1 and B2 FF's set. At the reset inputs of B1 and B2 FF's are AC gates, both enabled by C1 (TC13) time. When B2 is set, CB22 is False at O-164. TFD1 input to O-164 specifies B0 through B7 time, and will be False. When a count of 2 in B Counter at C1R1 time sets B2 FF, CB22 goes False and enables O-164. D input (TFD1) goes False to True at B8 time and this transition resets B1 and B2 FF's. With no sign pulse now in C1R1 time because reset of B1 and B2 cancelled the data setting in B, sign column of R1 indicates + (no sign) and sign of R1 has been changed.

ENABLE DISPLAY. Normally, when EPC goes to 0, PSZ3 becomes True and enables display. However, in a subtract when COF is set at Home time, a further step of complementing R1 and changing the sign occurs. Therefore display is not enabled until this is accomplished, even though EPC is at 0. This is controlled by ACOF1 applied to O-031 which develops PSZ3. When COF is set, which means R1 is to be complemented, ACOF1 at O-031 is True, therefore PSZ3 is False and will not enable display. The next Home time after complementing R1, COF resets, ACOF1 goes False and permits PSZ3 to go True, which, in turn, enables display.

Clamping of EPC to zero and reset of function FF's is exactly the same in EPC0 of subtract as in EPC0 of Add.

3. MULTIPLY FUNCTION

Multiplication can be described as a series of additions. Six multiplied by two can be described as: six added twice will give 12; or, two added six times will give 12.

In the EC-130, in a multiply operation, multiplication is done by adding the number in R1 to itself, digit by digit, a number of times that is specified by the number in R2.

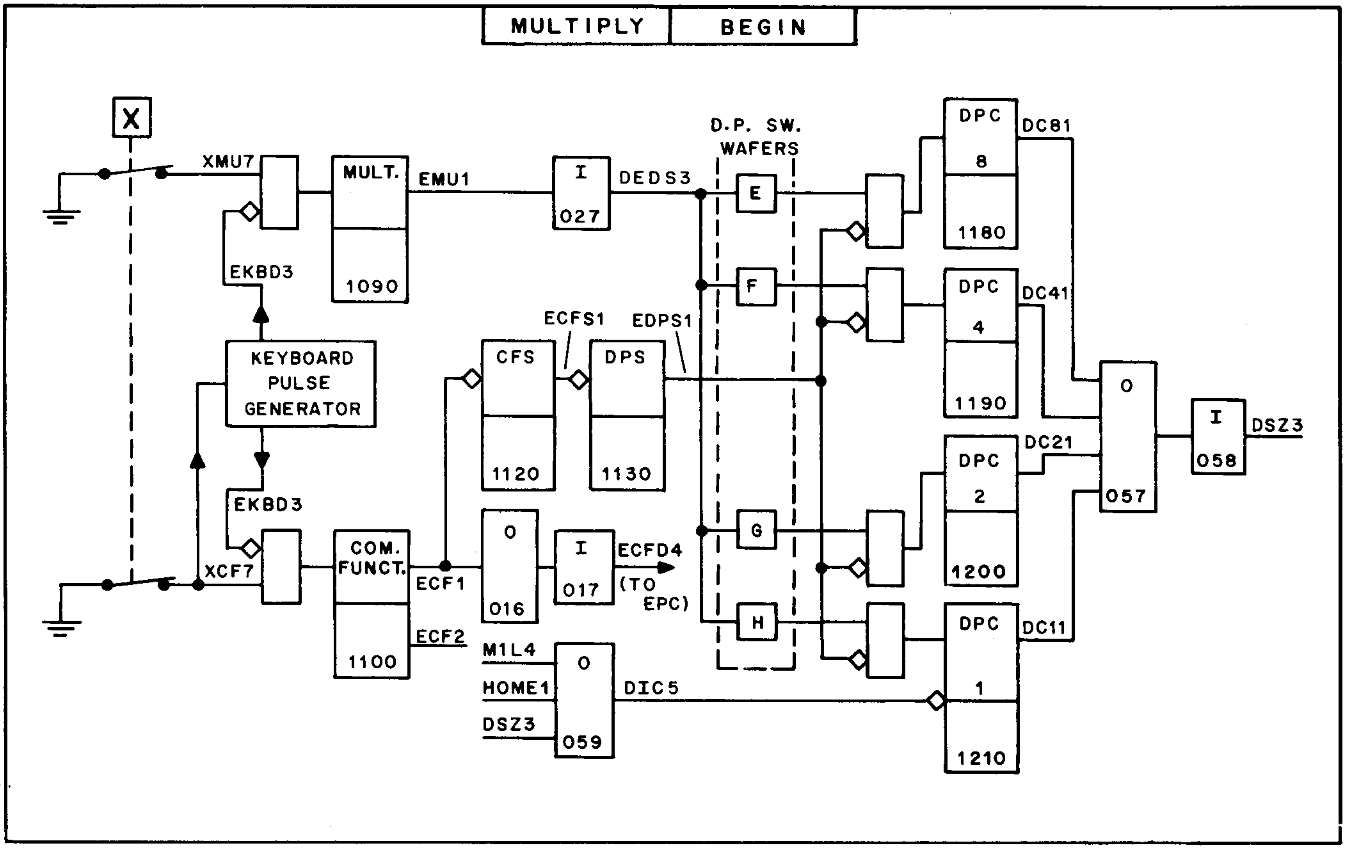
A multiply operation consists of shifting R1 to R0, thus clearing R1 for the add cycle; then shifting R2 left and using the MSD of R2 in D Counter to specify the number of times R0 (previous R1 data) will be added in R1. When that add cycle is completed, R1 is shifted left to multiply by 10, and the MSD of R1 is placed in D Counter. At the next shift R2 left, the MSD of R1 in D Counter becomes the LSD of R2. When all columns, C2 through C14, have been operated upon, the answer has been developed and the machine performs steps that place the whole answer in R2 and aligns the number around the decimal point. Then the answer is shifted down to R1 for display.

The machine is capable of displaying a 13-digit whole number answer. If the answer developed in the machine contains more whole number digits than the decimal position allows, the OVERFLOW LOCK lights, and the keyboard locks up preventing further operation.

MULTIPLY - BEGIN

The multiply function of the EC-130 is initiated by pressing Multiply (X) Key on the Keyboard after having placed the multiplier in Register two (R2) and the multiplicand in Register one (R1). It is not necessary to complete the entry in Register one by pressing ENTER Key because the first step of any function is Decimal Align, and that is all that the ENTER Key would accomplish.

SET FUNCTION. Pressing X Key closes multiply reed switch and, by means of an interlocking code bar, also closes Common Function (CF) reed switch. Closing Multiply Switch enables an AC gate at the set input of Multiply FF. Approximately 6 milliseconds later the Keyboard Delay (EKBD3) pulse, which is initiated by the closing of the CF reed switch, is applied as a + transition signal to the Multiply FF set input AC gate, and the transition sets Multiply FF. At the same time, closing of CF switch not only initiates EKBD3 signal but also enables an AC gate on the Set input of CF FF. EKBD3 signal is applied 6 milliseconds later to this AC gate, and the + transition sets CF FF.



UNCLAMP EPC. CF FF set output (ECF1) provides a + transition that sets Common Function Storage (CFS) FF if CFS is in a reset condition, which in turn sets Decimal Point Storage (DPS) FF. CFS will be reset only if the last operation performed at the keyboard was a number entry. If the number is not decimal aligned by ENTER Key, then the first step of any function is to Decimal Align. However, if the last operation at the keyboard was a function, then the number in R1 is already decimal aligned and CFS is set, therefore CF set cannot set CFS and no setting is placed into DPC. Also, the set output (True) of CF FF is applied through O-016 to I-017, and inverted False, designated ECFD4. Previous to the setting of CF FF, the set output (ECF1) was False, inverted True by I-017 and applied to diodes that clamped the EPC FF's to reset, which is EPC Zero. When CF is set, the False output of I-017 removes the clamping action of the diodes at the EPC FF's, and the next Home time steps EPC to 1.

SET DPC. Before Multiply FF is set, set output (EMU1) is False, and, inverted to True by I-027, is applied as an enable signal (DEDS3) through the decimal point switch wafers to AC gates at the set inputs of the Decimal (Point) Counter (DPC) FF's. Even though MULT. FF becomes set in Multiply, the AC gates at DPC FF's retain the "memory" of this enable (True) signal for a period of time (See Basic Logic discussion). The Decimal Point switch position determines which of the DPC FF AC gates are enabled. In this case, with the Decimal Point switch on 2, DPC8, DPC4, and DPC2 are enabled. (See DPC discussion.)

When DPS sets, the set output (EDPS1) False to True transition is applied at all DPC FF AC gates. Since only DPC8, DPC4 and DPC2 are enabled, only those DPC FF's set. Thus, the setting of DPC represents 14, and two more counts, or advances, are necessary to bring DPC to zero. This is the condition for Decimal Align with the decimal position switch on 2, and the decimal point position designating two places to the right of the decimal point.

MULTIPLY - EPC1

INHIBIT DISPLAY. When EPC steps off zero PSZ3 (I-032) goes False. PSZ3 is applied at A-225 in the Display Timing to enable display when True. Therefore, on any EPC step other than zero, Display is inhibited because PSZ3 is False. Display will not be enabled until PSZ3 again goes True, which will be at the end of the function.

DECIMAL ALIGN. The logic action in EPC step 1 is to decimal align the number in Register one. During Begin of Multiply function, DPC is set to the proper number for the decimal alignment. DPC counter setting specifies the number of columns that the digits in R1 will be shifted left in order to put the whole number portion of the entered digits to the left of the decimal point on the display.

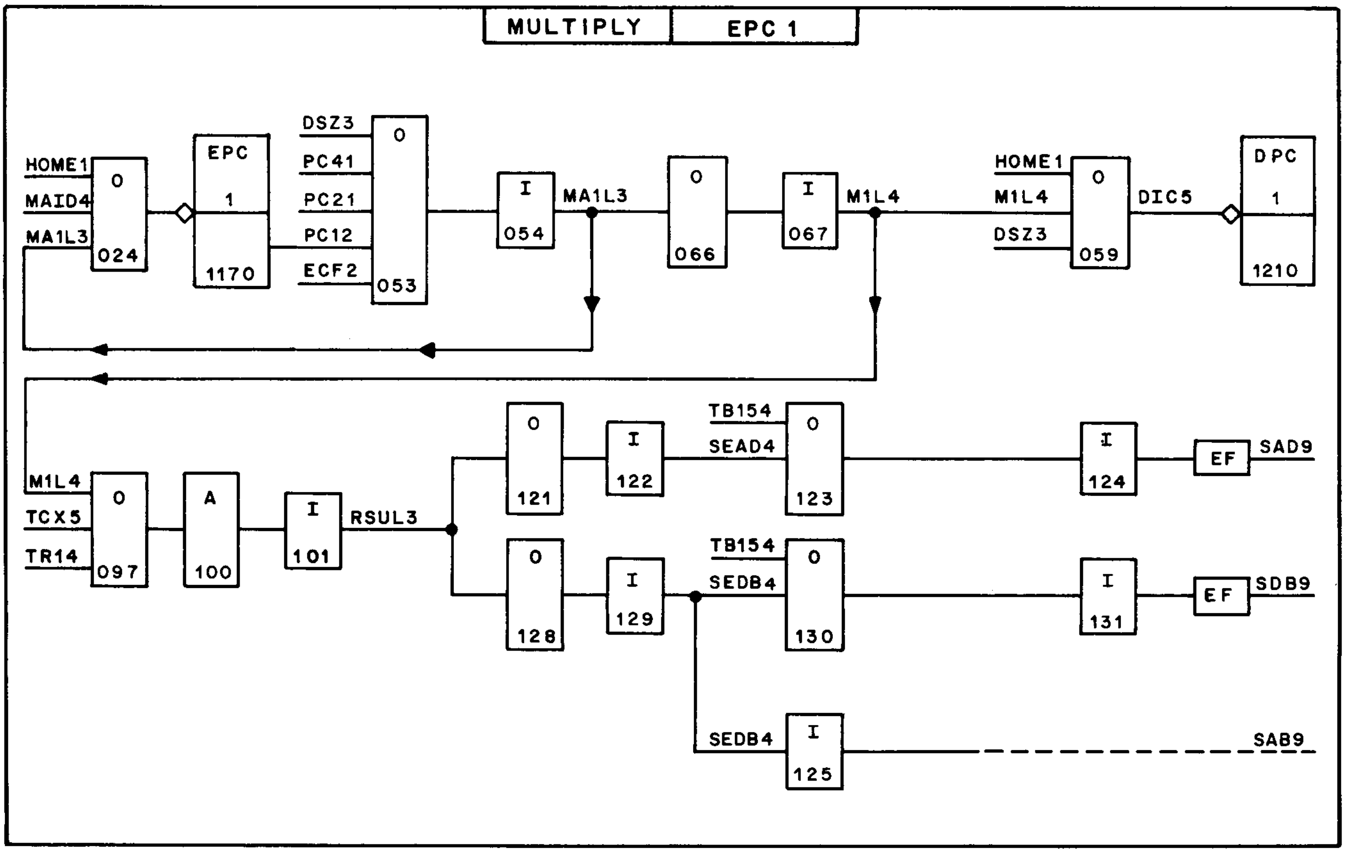
Setting of EPC1 FF causes reset output of EPC1 (PC12) to go False. This False output is applied to enable O-053. Because EPC2 and EPC4 are reset, PC21 and PC41 will be False. CF FF has been set by Mult (X) Key code bar interaction, thus CF reset output (ECF2) will be False. DSZ3 will be False because the Decimal Point Counter has been set to 14, thus it is not zero. Therefore, O-053 output will be False since all inputs are False.

False output of O-053 is inverted True by I-054, designated MA1L3. MA1L3 is applied back to O-024 to keep EPC on step 1. As long as there is a True input continuously present at O-024, HOME1 cannot step EPC. Until the gate is enabled again by MA1L3 going False, EPC stays on step 1. MA1L3 is also applied through O-066 to I-067 where it is inverted False, designated M1L4, and applied to enable O-097.

When all inputs to O-097 are False, the output will be False. This will occur during R1 time because of TR14, and during C2 through C14 time because TCX5 will be False during C2 through C14 time. Thus a False output is present from O-097 during R1 time from C2 through C14 time.

False from O-097 is applied through A-100 to I-101, inverted True, designated RSUL3, and applied through O-121 to inverter I-122 and inverted False, designated SEAD4. SEAD4 is applied to enable O-123. When TB154 is False, which will be every B15 time, the output of O-123 will be False and, applied to I-124, will be inverted True. The True output of I-124 is applied through an emitter-follower to the counters as SAD9. This means that, as long as SEAD4 is False at gate O-123, there will be an A to D shift every B15 time.

RSUL3 is also applied through O-128 to I-129 and inverted False, designated SEDB4. SEDB4 is applied to enable O-130. When TB154 is False, which will be every B15 time, the output of O-130 will be False, and applied to I-131, inverted True. True output of I-131 is applied through an emitter-follower to the counters as SDB9. This means that, as long as RSUL3 is True at gate O-128 there will be a D to B shift every B15 time.



SEDB4 is also applied to I-125, inverted True, and applied to O-126 as an inhibit signal so that there cannot be a shift A to B when there is a shift D to B. Two simultaneous inputs to the same counter is never desired, therefore, when shift D to B is called for, shift A to B is inhibited.

At the T-input of DPC1 FF, O-059 is enabled by M1L4 and DSZ3 both being False. Therefore, HOME1 can step DPC by 1 each Home time. Since DPC was set to 14, two Home times will step DPC to 0. When DPC steps to 0, DSZ3 (I-058) goes True and inhibits O-059.

After two Home times, which will mean two passes of R1 data through the counters, DPC will be stepped to Zero (since DPC was set to 14 for decimal align, in two more steps DPC becomes Zero). Each pass of R1 through the counters shifts R1 left by one column, thus two passes shifts R1 left by two columns, and completes Decimal Alignment.

When DPC goes to Zero, DSZ3 goes True. When DSZ3 goes True at O-053, this gate is inhibited and MA1L3 goes False. MA1L3 (False) at O-024 permits Home to step EPC to 2 by causing PIC5 to go True which resets EPC1, and the reset of EPC1 causes set of EPC2. At the same time, MA1L3 going False makes M1L4 True which, in turn, makes RSUL3 False. RSUL3 going False inhibits gates O-123 and O-130, which prevents any further shifts left.

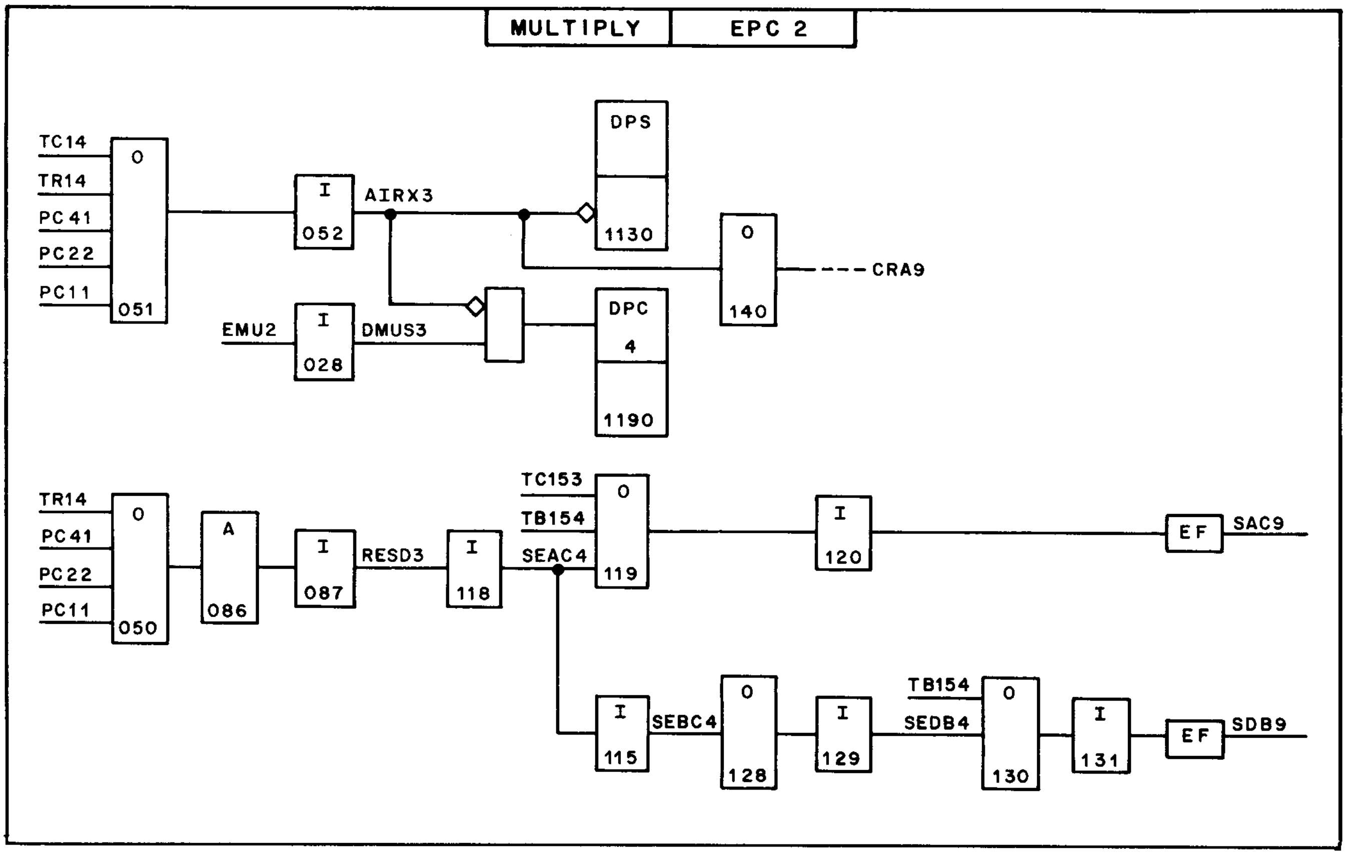
At the same time, M1L4 going True, as well as DSZ3 going True, at O-059 at the input of DPC1 FF prevents HOME1 from any further stepping of DPC, and DPC remains at zero.

This completes Decimal Alignment during EPC step 1 of multiply function.

MULTIPLY - EPC2

SET DPC TO 4. When EPC steps to 2, PC11, PC22, and PC41 are all False at O-051. The other inputs to the gate are TC14 and TR14, which will be False during C1 time and R1 time. Thus, the output of O-051 will be False during C1R1 time because all inputs are False. O-051 False output is inverted True by I-052, designated AIRX3. AIRX3 is applied as a positive transition to an AC gate at the set input of DPC4 FF. This AC gate is enabled by the output of I-028, designated DMUS3. EMU2 at I-028 is False because Mult. FF is set in Multiply. EMU2, inverted True by I-028 (DMUS3), is applied to enable DPC4 FF AC gate. (See DPC discussion.)

At the end of EPC step 1, DPC was zero, which meant all FF's were reset. At EPC step 2, the positive transition (AIRX3) at DPC4 FF AC gate will set DPC4 FF. This represents a count of 4 in the DPC, and it will take 12 more counts into the DPC to bring the counter to zero. Therefore, DPC can control 12 column shifts left of R1 data.



RESET DPS. The False to True output transition of I-052, designated AIRX3, is also applied to reset DPS FF at this time.

COMPARE SIGNS. During EPC2, the sign of the answer is determined by adding the signs of R1 and R2. This is accomplished by inhibiting (blocked) reset of A Counter (CRA9) at the end of C1R1 time. AIRX3 is True during EPC2 and C1R1 time and at O-140 will inhibit CRA9, which would normally occur at the end of C1R1 time. AIRX3 True makes CRA9 False, thus no reset of A Counter.

If both signs are +, there is no sign pulse in either C1R1 or C1R2, therefore no change in sign. If both signs are negative, however, there is a sign pulse in C1R1 and C1R2. The blocking of CRA9 leaves A set to 1 by C1R1 sign pulse. Then C1R2 counts "on top" of the 1, and A Counter sets to 2. The next A to B shift places this 2 setting in B Counter. A count of 2 in B Counter during C1 time is used to enable logic gates that reset B to 0, which removes the sign pulse from C1R2 (See Change Sign discussion). Thus, if signs of R1 are the same, either both + or both -, the sign of C1R2 will be + (no sign pulse in C1R2).

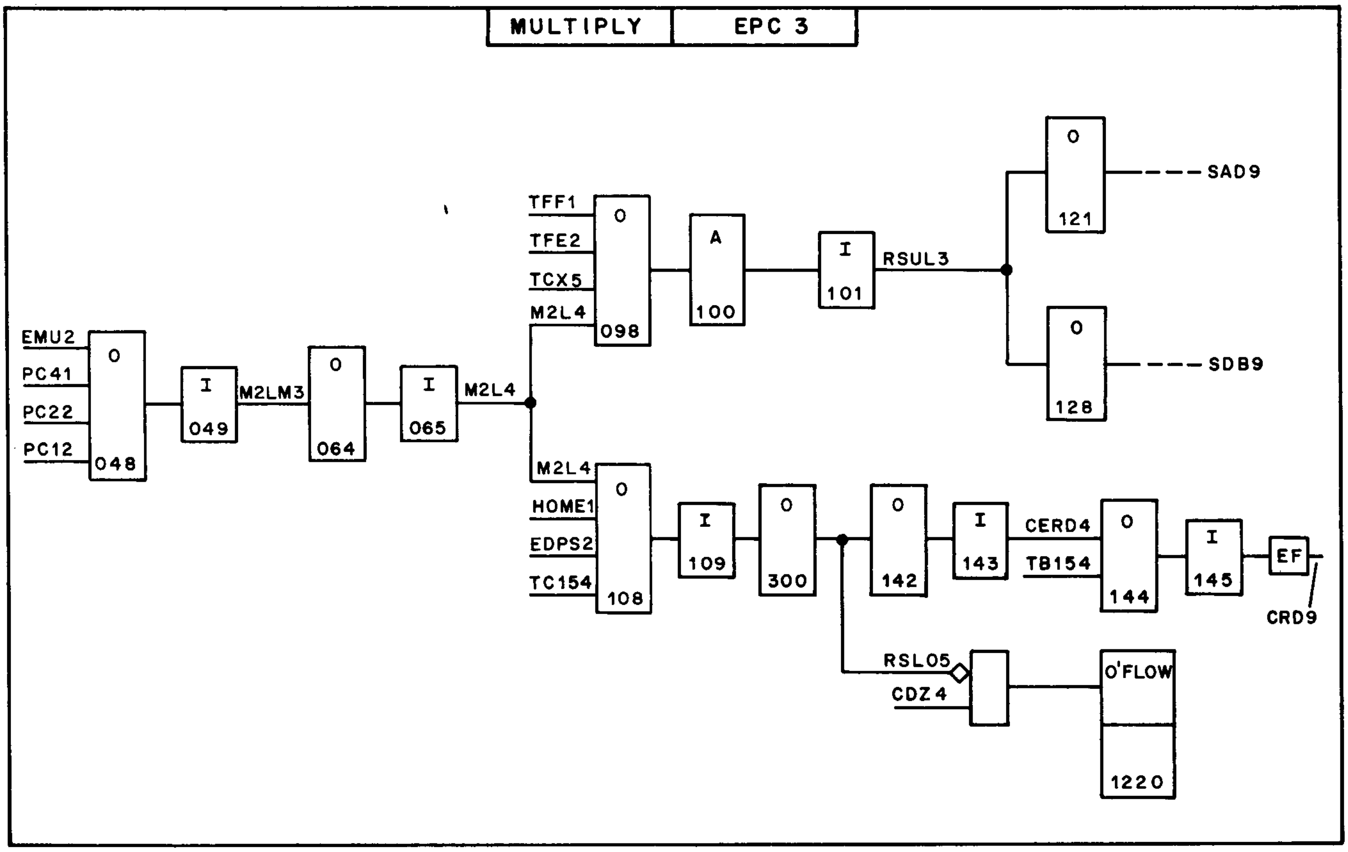
If C1R1 is negative, A Counter sets to 1. Inhibit of CRA9 leaves this 1 in A and C1R2 counts on top. If C1R2 is +, there is no sign pulse and A remains at 1, and this becomes the sign of C1R2, and R2 sign is negative. If C1R1 is +, inhibit of CRA9 leaves A set to 0, (no sign pulse in C1R1) and C1R2 counts on top. If C1R2 is negative (sign pulse in C1R2) A sets to 1, this becomes the sign of C1R2, and R2 sign is negative. Thus, if the signs of R1 and R2 are not the same, the sign of C1R2 will be negative.

SHIFT DOWN R1 TO R0. Since all arithmetical functions of the EC-130 are performed with one of the numbers being in R0 time, the contents of Register 1 (R1) are shifted to R0. This represents a "Shift Down" operation and is controlled by O-050. PC11, PC22, and PC41 at the input specify EPC step 2, and are False during EPC step 2. TR14 will be False during R1 time, and the output of O-050 will be False during R1 time. False output of O-050 is applied through A-086 to I-087 and inverted True, designated RESD3. RESD3 is inverted False by I-118 (SEAC4) and applied to enable O-119. The other inputs to O-119 are TB154 and TC153. TC153 is False during all C times except C15, thus is False from C1 through C14 time. Therefore, the output of O-119 will be False each B15 time from C1 through C14 as long as SEAC4 is False. False output of O-119, inverted True by I-120, is applied through an emitter-follower as SAC9 to the counter circuits to initiate as A to C shift of data every B15 time at R1 time during C1 through C14 time.

False output of I-118 (SEAC4), inverted True by I-115, designated SEBC4, is applied through O-128 to I-129, and inverted False. The output of I-129, designated SEDB4, enables O-130. The other input to O-130 is TB154, which means there will be a False output from O-130 every B15 time as long as SEDB4 is False. False output of O-130, inverted True by I-131, is applied through an emitter-follower as SDB9 to the counter circuits to initiate a D to B shift each B15 time at R1 time during C1 through C14 time.

The result of the A to C shift is to move R1 data into R0 time, which puts significant data into R0 for use in the arithmetical process. The D to B shift places zeros in R1 time, thus effectively clearing R1 for later arithmetical use.

The logic action in EPC step 2 takes place during one pass of data through the counters. At the next Home time at gate O-024, EPC steps to 3.



MULTIPLY - EPC3

SHIFT R2 LEFT. A primary logic function in EPC step 3 is to shift R2 left. At this shift left, data in D Counter will be placed in the LSD position of R2, and data in the MSD position of R2 will be placed in D Counter.

When EPC steps to 3, PC12, PC22, and PC41 are all False and will enable O-048. Another input to O-048 is reset output (EMU2) of Mult. FF, which is False during multiply. The output of O-048 is False and, inverted True by I-049, designated M2LM3, is applied through O-064 to I-065 and inverted False. False output of I-065, designated M2L4, is applied to enable gates O-098 and O-108.

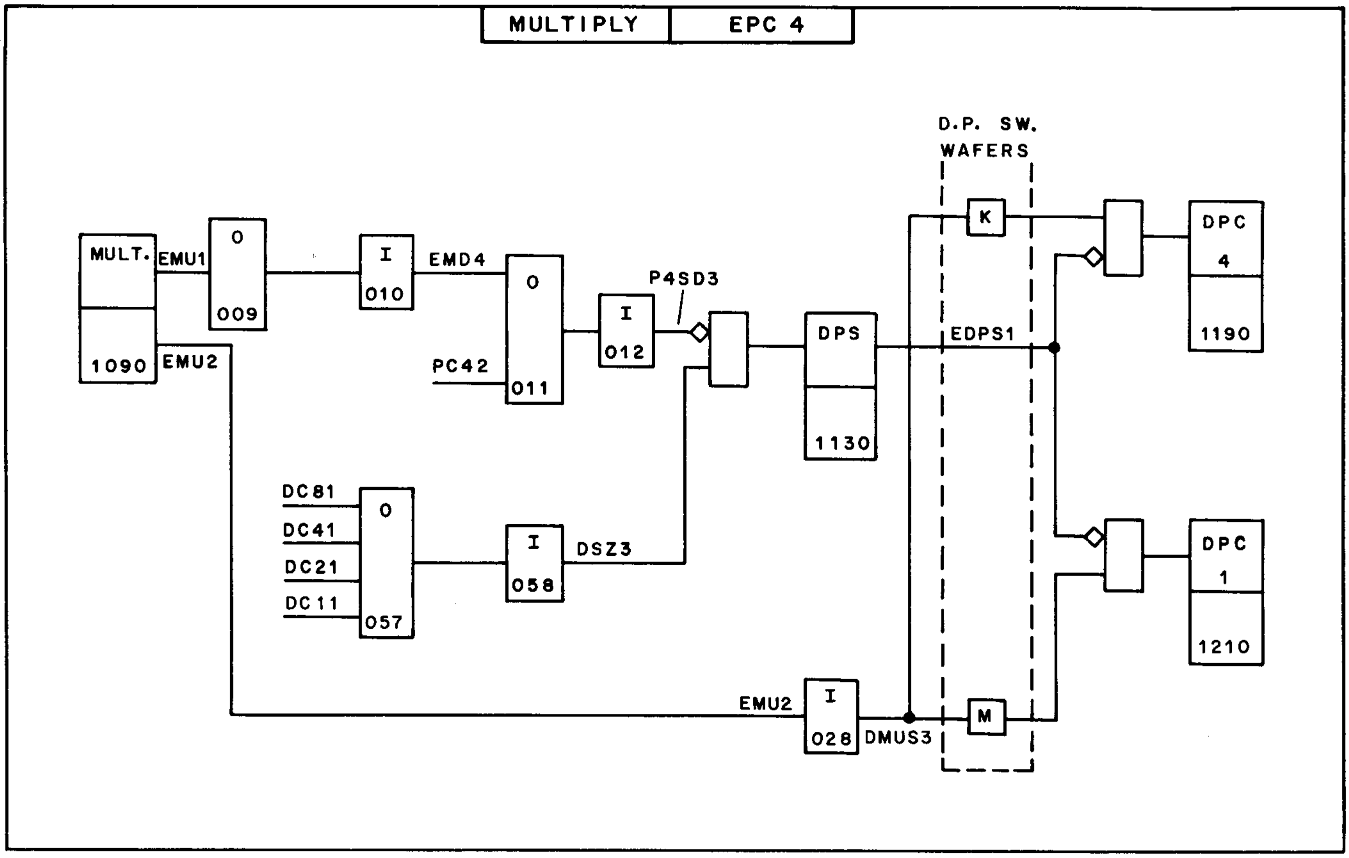
Gate O-098 is enabled by M2L4 and, when all other inputs are False, the output is False, TFE2 and TFF1 inputs specify R2 time, and TCX5 specifies C2 through C14 time (when not in a divide function). This means that there will be a False output from O-098 during EPC step 3 in multiply for all R2 times during C2 through C14 times. False output of O-098 is applied through A-100 to I-101 and inverted True, designated RSUL3. RSUL3 is applied through O-121 and O-128 to shift R2 data left at B15 time exactly as R1 was shifted left in EPC step 1, Decimal Align.

RESET D. M2L4 is also applied as an enable signal to O-108. The other inputs to O-108 are HOME1, EDPS2 and TC154. This means that during a shift 2 left, at C15 time if DPS is set, TC154 going False will cause a False output from O-108.

HOME1 has no logic function at this gate (O-108), but provides a faster rise time of the output for a more effective triggering signal. False output of O-108, inverted True by I-109, is applied through O-300 (RSLO5) and O-142 to I-143 and inverted False, designated CERD4. CERD4 enables O-144, whose other input is TB154. This means that at B15 time, if RSLO5 is True, the output of O-144 will be False. False output of O-144, inverted True by I-145, is applied through an emitter-follower as CRD9 to reset D Counter to zero to ensure that no data is left in D Counter.

SET OVERFLOW. At the same time, RSLO5 False to True transition is applied to an AC gate at the set input of Overflow FF. The enable on this AC gate is CDZ4, and if CDZ4 is True this specifies that there is significant data in D Counter and there are no more columns to shift R2 into, which indicates an answer too large for machine capacity (an overflow condition) this Overflow FF sets.

At the next HOME1 True, PIC5 at the input of EPC1 FF will step EPC to 4.



MULTIPLY - EPC4

In EPC4 of Multiply, if DPC is zero (DSZ3 True), the Decimal Point Counter sets to a number that is determined by the position of the Decimal Point Switch. In this case, decimal position 2 has been chosen.

SET DPC. EMD4 (I-010) output is False because Mult. FF is set. EMD4 is applied to enable O-011. The other input to O-011 is PC42, which will be False, specifying EPC step 4, and the output of O-011 will be False and inverted True by I-012, designated P4SD3. P4SD3 False to True transition is applied to an AC gate at the set input of DPS FF.

The enable on this AC gate is DSZ3, which will be True if the Decimal Point Counter has been stepped to zero by the counting down of DPC in EPC step 6 of the multiplication loop. When DSZ3 is True and EPC steps to 4, the positive transition from I-012 (P4SD3) sets DPS FF, (which was reset in EPC step 2).

At this time, Mult. FF being set has established the reset output (EMU2) of Mult. FF at False. EMU2, inverted True by I-028, designated DMUS3, is applied through the Decimal Point Switch wafers to enable AC gates on the set side of the DPC FF's. The position of the Decimal Point Switch determines which of the AC gates will be enabled, in this case DPC1 and DPC4.

When DPS sets at EPC4 because DSZ3 is True, EDPS1 goes False to True and, applied to the AC gates of the DPC FF's, will set FF's 1 and 4, which have been enabled by DMUS3 through the Decimal Point Switch wafers. DPC1 and DPC4 being set establishes DPC set to 5, which means that it will take 11 more counts, or advances, for the DPC to return to zero. This conforms to the decimal point position being at two, since there are 11 columns to the left of the decimal point. 5 is the 16's complement of 13 minus the decimal point setting (2).

This completes action in EPC step 4 and, at the next HOME1 True at O-024, PIC5 will step EPC to 5.

MULTIPLY - EPC5

COF SET? COF will set at HOME1 if Carry FF is set because ACRY1 True enables an AC gate (1241) on COF FF. Carry FF will be set at HOME1 if the last column (C14) add cycle produces a carry. C14R1 add cycle will produce a carry if A Counter counts past 9.

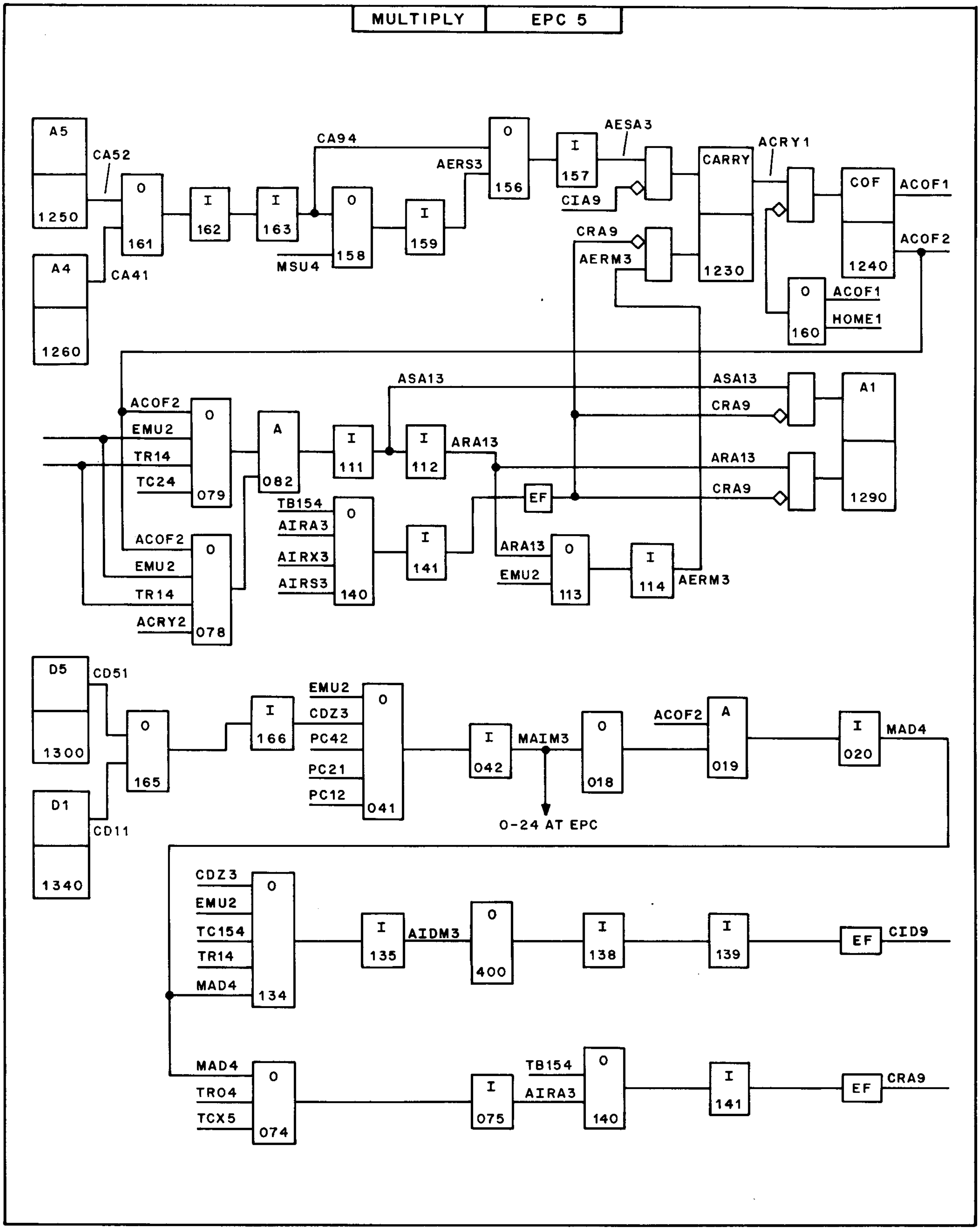
Carry FF set, thus COF set, is controlled by O-161. A Counter FF's A4 (CA41) and A5 (CA52) outputs are applied to O-161. When A Counter reaches 9, meaning A5 set - A4 reset, CA41 and CA52 outputs will be False, and the output of O-161 will be False. Inverters I-162 and I-163 perform a double inversion and the output of I-163 will be False, designated CA94, CA94 is applied to O-156, and also to O-158. Another input to O-158 is MSU4 which is False in a subtract function, which means it will be True in Multiply. The output of O-158 will be True when any input (MSU4) is True and, inverted False by I-159, is applied as a False input to O-156. Since both inputs to O-156 are False, the output is False and, inverted to True by I-157, designated AESA3, is applied to enable an AC gate (1232) at the set input of Carry FF. The next CIA9 pulse at the AC gate of the Carry FF, which is also the pulse which resets A5 FF, sets Carry FF. This indicates that A Counter has counted to 10 and there is a carry of one.

Carry FF set output (ACRY1) enables an AC gate at the set input of COF FF. The positive transition signifying Home time (HOME1) is applied as the other input to the AC gate and sets COF FF at Home time if Carry FF is set. COF being set enables logic that will add 1 to R2, which takes care of the carry of one by adding 1 to the LSD of R2.

ADD 1 TO R2. The inputs to O-079 specify a False output when COF is set (ACOF2); in multiply (EMU2); and during C2R1 time (TC24, TR14). O-079 False output is applied through A-082 to I-111, inverted True, designated ASA13, and applied to enable an AC gate at A1 FF set input. When A Counter is reset by CRA9 at the end of C2R1 time, A1 sets instead of becoming reset. Thus, A Counter starts from a count of 1 (1 has been added to A just before C2R2 time). Since C2R2 is the LSD of R2, 1 is added to LSD of R2.

SPECIAL CASE. However, suppose C2R2 data is already 9. The "add 1 to R2" would cause A to count past 9 when R2 data is 9, which would immediately set Carry and enable "add 1 to A" until Carry became reset again at Home time. Therefore, O-078 is enabled by ACOF2 and ACRY2, as well as EMU2 and TR14. If "ADD 1 to R2" results in Carry FF being set because A counted past 9, O-078 False output is applied through A-082 to I-111, and results in an "ADD 1 to R2" and also resets Carry immediately through I-112 (ARA13). ASA13 True enables A1 FF set. ASA13 True inverted False by I-112, designated ARA13, enables O-113. EMU2 at O-113 will be False in Multiply. O-113, acting as a negative AND will have a False output when ARA13 is False in Multiply. O-113 False, inverted True by I-114, designated AERM3, enables an AC gate (1236) on Carry FF reset input. When CRA9 goes True, which is when 1 is added to A Counter by the action of CRA9 and ASA13 at A1 FF, the same CRA9 resets Carry immediately. Thus, under this special case logic, the results of adding 1 to A Counter when R2 is already at 9 is taken care of for the Add and reset of Carry in a Multiply function.

RESET CARRY. Carry becomes reset by the same HOME1 that sets COF. However, COF set adds 1 to R2. If C2R2 data should be 9, this would set Carry, which would add 1 to the next column. To reset Carry at this time, AC gate 1236 is enabled by AERM3 True. ASA13 True, which is developed to Add 1 to R2 is inverted False by I-112, designated ARA13, and is one input to O-113 acting as a negative AND. EMU2 will be False at O-113 since function is Multiply and Mult. FF is set, and O-113 output will be False. O-113 False, inverted True by I-114, designated AERM3 (enable reset in Multiply) enables AC gate 1236 on Carry FF. Thus CRA9 can reset Carry. The only purpose of AC gate 1236 is if a carry would propagate through R2, there is a means of resetting Carry before the next HOME1 time.


MULTIPLY
EPC 5
A5
1250
CA52
A4
1260
CA41
O
161
I
162
I
163
CA94
O
158
MSU4
I
159
AERS3
O
156
I
157
AESA3
CIA9
CARRY
1230
ACRY1
CRA9
AERM3
COF
1240
ACOF1
ACOF2
O
160
ACOF1
HOME1
ACOF2
EMU2
TR14
TC24
O
079
A
082
I
111
ASA13
I
112
ARA13
ASA13
CRA9
A1
1290
ARA13
CRA9
EF
TB154
AIRA3
AIRX3
AIRS3
O
140
I
141
ARA13
EMU2
O
113
I
114
AERM3
ACOF2
EMU2
TR14
ACRY2
O
078
D5
1300
CD51
D1
1340
CD11
O
165
I
166
EMU2
CDZ3
PC42
PC21
PC12
O
041
I
042
MAIM3
0-24 AT EPC
O
018
ACOF2
A
019
I
020
MAD4
CDZ3
EMU2
TC154
TR14
MAD4
O
134
I
135
AIDM3
O
400
I
138
I
139
EF
CID9
MAD4
TR04
TCX5
O
074
I
075
TB154
AIRA3
O
140
I
141
EF
CRA9

D COUNTER ZERO? At gate O-041 all inputs will be False in a multiply function at EPC step 5 if CDZ3 is False. CDZ3 will be False if D Counter has not reached zero setting. Since D Counter holds the multiplier in a multiply problem, D Counter setting delineates the progress of the problem. Counters D1 and D5 will both be reset if D Counter is zero. If either D1 and D5 are set, which will be true of any number other than zero, one of the set outputs will be True, and, applied to O-165, the output will be True. O-165 True output, inverted by I-166 will be False, designated CDZ3 and is applied to enable O-041.

ADD R0 TO R1. If all inputs to O-041 are False the output will be False. PC12, PC21, and PC42 will be False because the multiply function is in EPC step 5, and EMU2 will be False because Mult. FF is set. Therefore, O-041 output will be False and, inverted True by I-042, designated MAIM3, is applied through O-018 to A-019. If both inputs to A-019 are True the output will be True. The other input is ACOF2, which will be True unless Carry Overflow FF is set. The output of A-019 is inverted False by I-020, designated MAD4.

MAD4 False is applied to enable O-074. When all inputs to O-074 are False, the output is False. TCX5 will be False from C2 through C14 time. TR04 will be False during R0 time. Thus, during R0 time from C2 through C14 time, as long as MAD4 is False, O-074 output will be False. O-074 False output, inverted True by I-075, designated AIRA3, is used to inhibit O-140, thus no CRA9 at ROB15 time. CRA9 when True resets A Counter. When CRA9 is False, A Counter is not reset. If CRA9 is inhibited, then R0 data setting is retained in A Counter and R1 data is counted into A "on top" of R0 data. This is an integral part of an Add or Multiply function, and is specified as "Add R0 to R1".

COUNT D DOWN 1. MAD4 False also enables O-134. The other inputs to O-134 specify that when D Counter is not zero (CDZ3 False) and the function is Multiply (EMU2), at C15R1 time (TC154, TR14) the output of O-134 will go False. False output of O-134, is inverted True by I-135, designated AIDM3. AIDM3 is applied through O-400 to I-138 and double inverted by I-138 and I-139, ending up True. True output of I-139 is applied through an emitter-follower as CID9 to the counter circuits to "increment D Counter by 1". Since D Counter is a down counter, this effectively counts D down by 1.

STEP EPC. Home is prevented from stepping EPC beyond 5 by the presence of MAIM3 True, at gate O-024 of EPC. When any input to O-024 is already True, the introduction of another True signal, in this case HOME1, cannot cause an EPC step. Therefore, EPC remains on 5 and goes continually through the functional logic of EPC step 5 until MAIM3 goes False at O-024 and allows HOME1 to step EPC to 6. MAIM3 will go False when D Counter, after being stepped down by one each "Add R0 to R1" cycle, goes to zero. Then CDZ3 at O-041 goes True, which in turn makes MAIM3 False, and the next HOME1 time will step EPC to 6.

MULTIPLY - EPC6

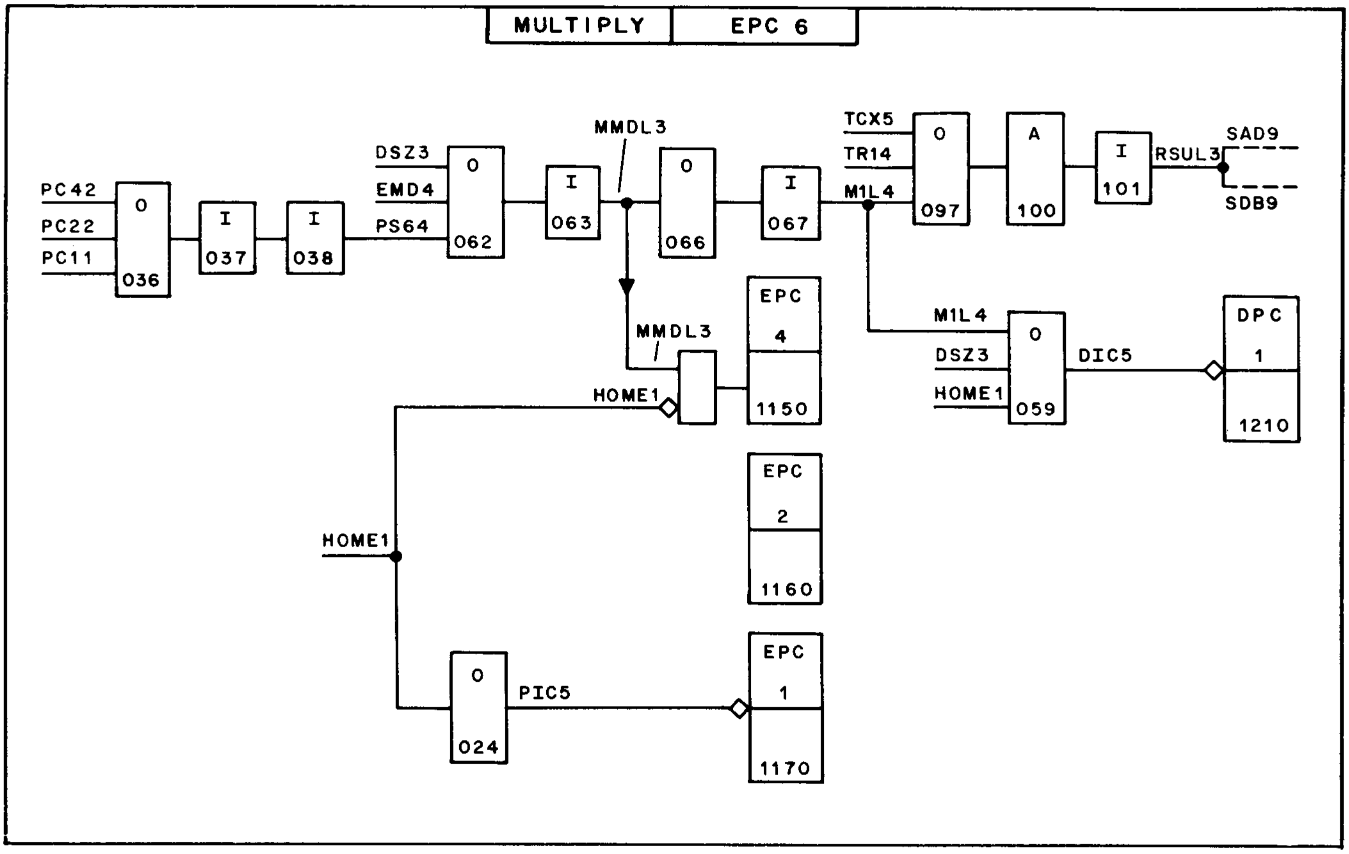
In EPC step 5, R0 was added to R1 and DPC counted down 1, which placed D Counter to zero and enabled EPC step to 6. However, when R0 was added to R1, a carry may have developed which would set COF at the end of EPC5. When COF is set, this indicates an addition of 1 to R2. This is accomplished exactly as described in EPC step 5.

The next logic function in EPC step 6 is to test DPC for zero. This is done at O-057 exactly as in EPC step 4. If DPC is zero, EPC steps to 7 with no further logic action. If DPC is not zero, meaning the arithmetic is not complete, then R1 is shifted left, DPC counted up 1, and an EPC return step to EPC3 is performed.

SHIFT R1 LEFT. If the other inputs to O-062 are False, the output will be False. PS64 will be False because the multiply function is in EPC step 6, and EMD4 will be False because function is multiply.

The False output of O-062, inverted True by I-063, designated MMDL3, is applied through O-066 to I-067, and inverted False, designated M1L4. O-097 is enabled by M1L4 and, during R1 (TR14) time from C2 through C14 time (TCX5), the output is False and applied through A-100 to I-101 is inverted True, designated RSUL3. RSUL3 is used to control R1 shifts left exactly as this signal was used to control R1 shifts left in Decimal Align of EPC step 1.

COUNT DPC UP 1. M1L4 also enables O-059 at DPC1. If DPC is not zero, DSZ3 will be False and, at Home time, DPC will be counted up by one by HOME1 going True.



STEP EPC6 to 3. MMDL3 (I-063) enables an AC gate at the reset input of EPC4 FF, and will be True during EPC step 6. Thus, the same Home time that counts DPC down by one will step EPC from 6 to 3. Usually, Home time would step EPC to 7, which would be all FF's set. However, the AC gate at EPC4 FF reset input which is enabled by MMDL3 will reset EPC4 FF. This results in EPC1 set, EPC2 set and EPC4 reset, which is EPC step 3. Machine logic functions then progress from EPC step 3 to EPC step 6 then back to EPC step 3 until DPC finally reaches zero.

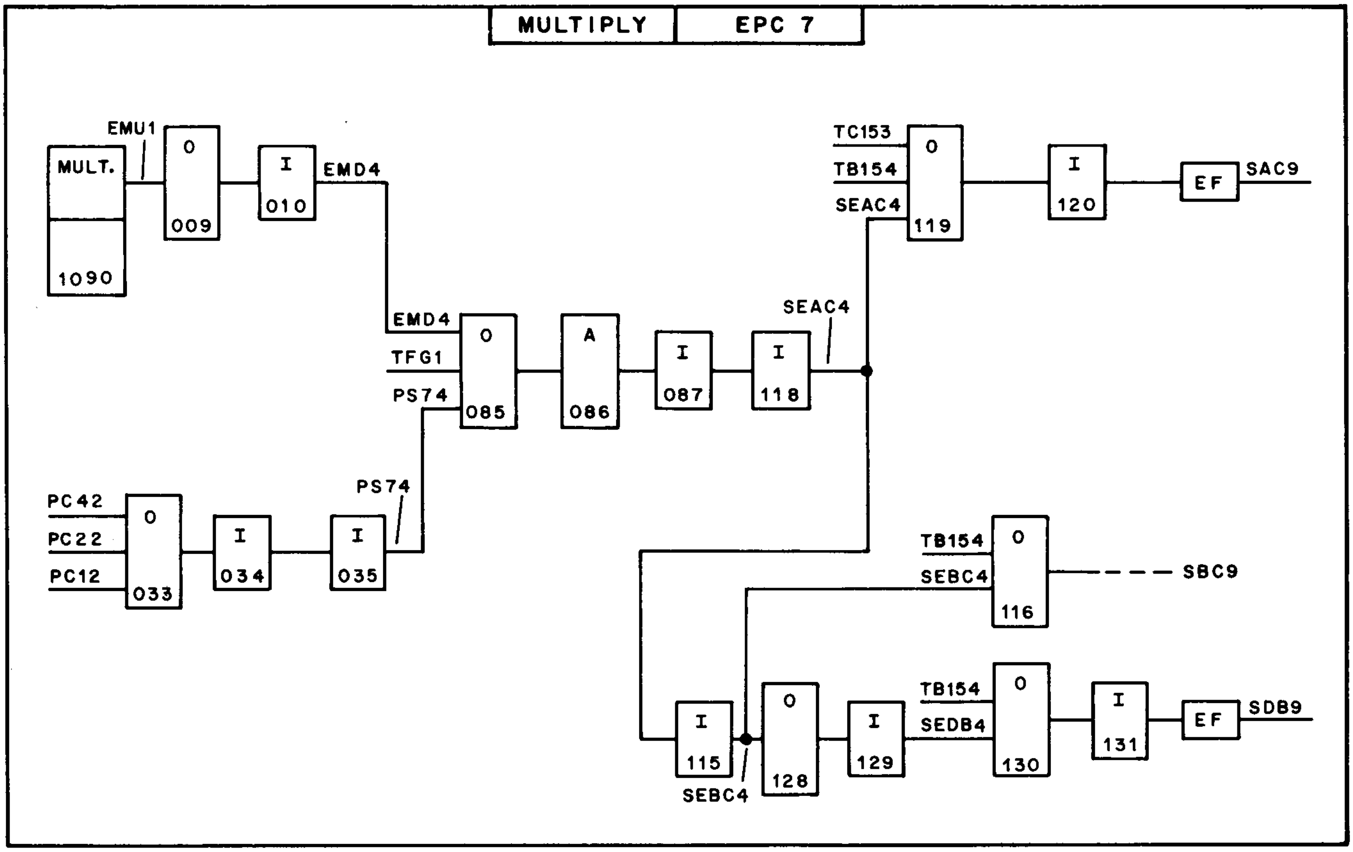
STEP EPC6 to 7. When DPC reaches zero, DSZ3 will be True at O-062 and MMDL3 goes False, which inhibits the AC gate at EPC4 FF. The next Home time, then, steps EPC to 7. Therefore the DPC setting determines whether EPC steps 6 to 7 or 6 to 3, and, at the same time, controls the number of shifts left.

MULTIPLY - EPC7

When EPC step 7 is reached, it means that the multiply logic has completed the answer and the answer is decimal aligned in R2. Since R1 is the answer display register, the multiplication product must be shifted to R1, which is a "shift down" process.

SHIFT DOWN. PS74, developed by I-035, enables O-085. EMD4 (I-010) will be False because machine function is Multiply. During R1 through R4 time, which is specified by TFG1 at O-085, O-085 will have a False output, which is applied through A-086 and double inverted by I-087 and I-118, ending up as a False input (SEAC4) at O-119. The other inputs to O-119 specify that during all C times other than C15 (TC153), the output of O-119 will be False every TB154 time. False output of O-119, inverted True by I-120, is applied through an emitter-follower to the counters as SAC9, which causes an A to C shift each B15 time.

At the same time, False output of I-118, designated SEAC4, inverted True by I-115, designated SEBC4, is applied through O-128 to I-129, inverted False (SEDB4) and applied to enable O-130. The other input to O-130, TB154, specifies that each B15 time there will be a False output from O-130. False output of O-130, inverted True by I-131, is applied through an emitter-follower to the counters as SDB9, which causes a D to B shift each B15 time.



SEBC4 True applied to O-116 also inhibits an A to B data shift when a D to B data shift is called for by the machine logic, since simultaneous shifts of data from two sources into the same counter is never desired.

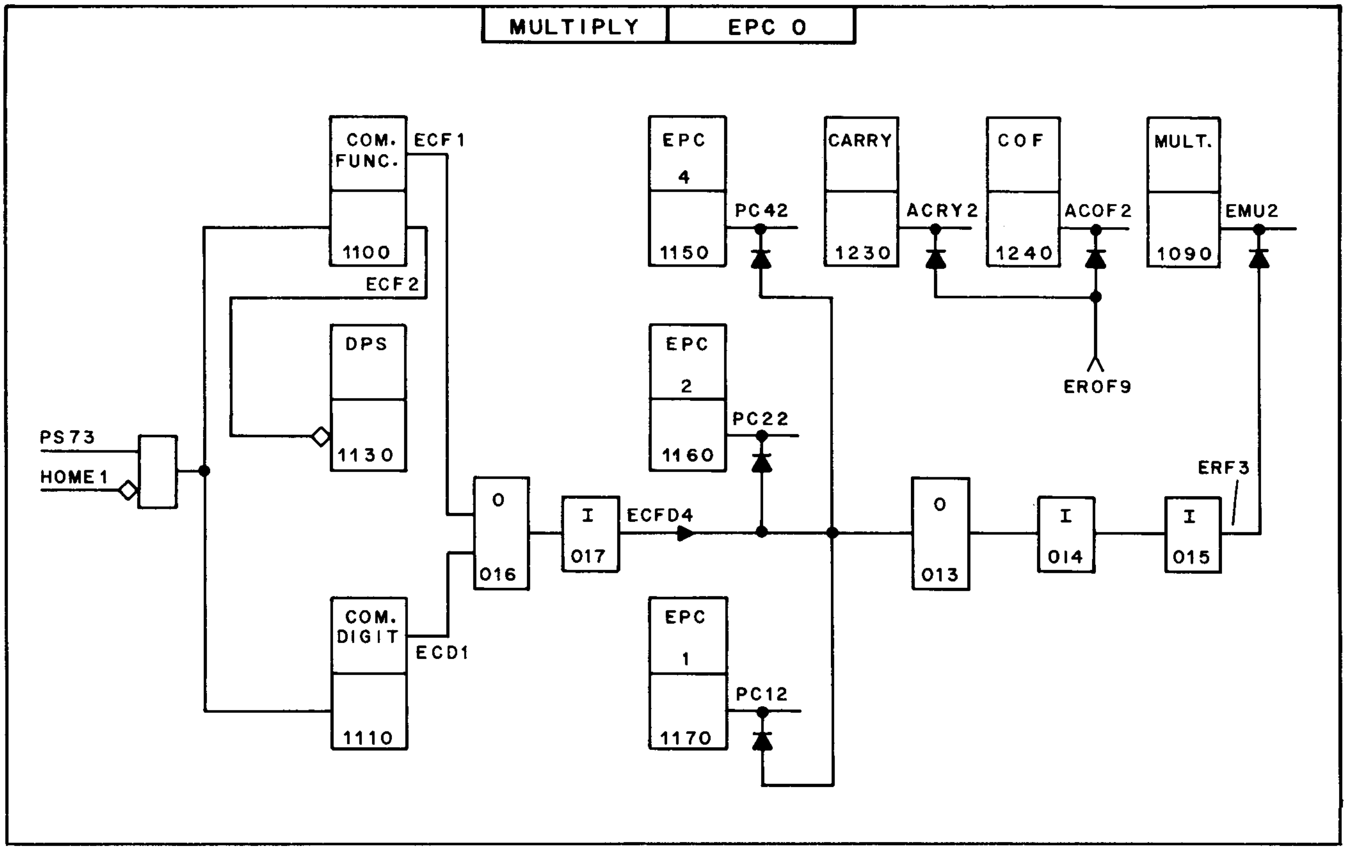
Simultaneously with the development of the shift down signals, PS73 is applied to enable an AC gate at reset inputs of both CF and CD. The other input to the AC gate is HOME1, and at the first Home time after EPC step 7, CF resets (CD was not set in Multiply), and the same HOME1 on O-024 at EPC1 FF steps EPC to zero.

MULTIPLY - EPC0

CLAMP EPC TO 0. The inputs to O-016 are ECF1 and ECD1. When CF resets at the end of EPC step 7, ECF1 goes False. Since CD is reset, ECD1 is False, and the output of O-016 is False. False output of O-016, inverted True by I-017, designated ECFD4, is applied to clamping diodes on EPC FF reset outputs, and clamps EPC to zero.

RESET FUNCTION FF's. The False to True output transition of I-017 (ECFD4) is applied through O-013 to I-014, double inverted by I-014 and I-015, ending up as a False to True transition (+transition) at I-015 output, designated ERF3. ERF3 is applied to reset any function FF's that are set, in this case Multiply.

ENABLE DISPLAY. When EPC steps to zero, display is enabled by PSZ3 going True at A-225 in the Display Logic when EPC goes to 0, and multiply function is complete.



4. DIVIDE FUNCTION

Division can be considered a series of subtractions, thus 36 divided by 12 could be described as "How many times can 12 be subtracted from 36," and the answer is 3. Subtraction, in turn, can be done by means of complementary addition. Thus, 3 subtracted from 6 could be arrived at by adding the complement of 3, which is 7, to 6 with the answer appearing to be 13. However, taking the complement of 3 stipulates a borrow of one, and the addition of 7 and 6 produces a carry of one. The carry cancels the borrow, and the answer is 3, exactly as would be arrived at by a more usual subtract.

In the EC-130, the arithmetical process of subtraction is carried out by complementary addition. Since division is a series of subtractions, division involves complementary addition with the necessary shifts of the number to the left at appropriate times to establish decimal positioning.

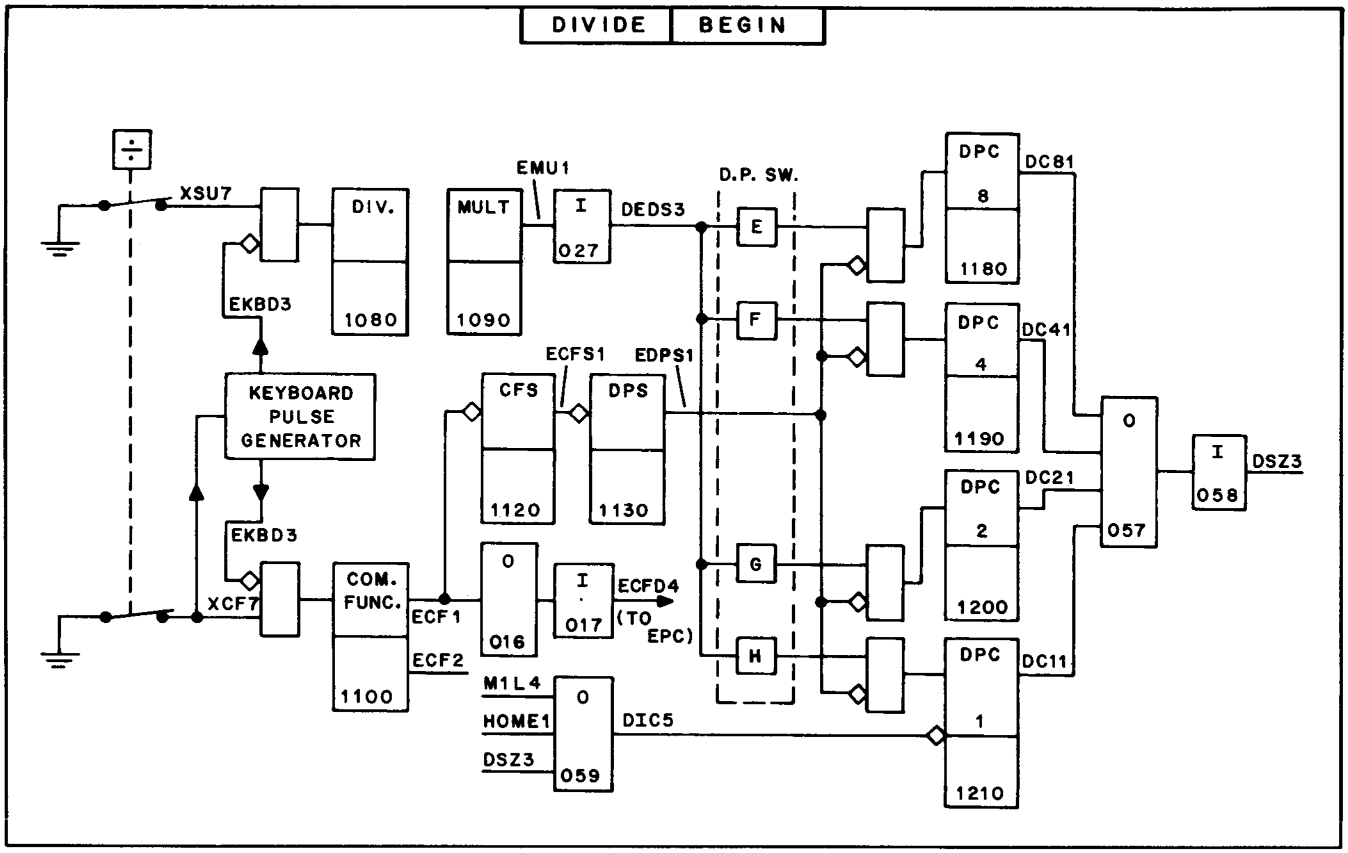
In a divide operation, R2 is shifted digit by digit into R1 via D Counter until enough of R2 is in R1 for a successful subtract to take place. For each successful subtract (no overdraft), 1 is added to the LSD of R2. After all possible successful subtracts have been accomplished for this step, another shift left of R2 places the next decimal place into R1, and more subtracts attempted. Again, for each successful subtract 1 is added to the LSD of R2. Meanwhile, the last R2 left shift moved the number representing the first set of successful subtracts one place to the left. The answer, in the form of successful subtracts accomplished, is accumulated in R2, then shifted down to R1 to appear as the answer when the display unblanks.

As in multiply, an answer beyond the capacity of the machine to display will light OVERFLOW LOCK. Additionally, a problem that is impossible to solve, such as a zero divided by zero, will keep the machine in an operational loop that prevents the display from being unblanked.

In the following detailed discussion of Divide Function, the discussion is referenced to the Divide Function Logic Chart.

DIVIDE - BEGIN

The divide function of the EC-130 is initiated by pressing Divide (÷) Key on the Keyboard after having placed the dividend in R2 and the divisor in R1. It is not necessary to complete the entry in R1 with the ENTER Key because the first step of any function is Decimal Align, and that is all the ENTER Key would accomplish.

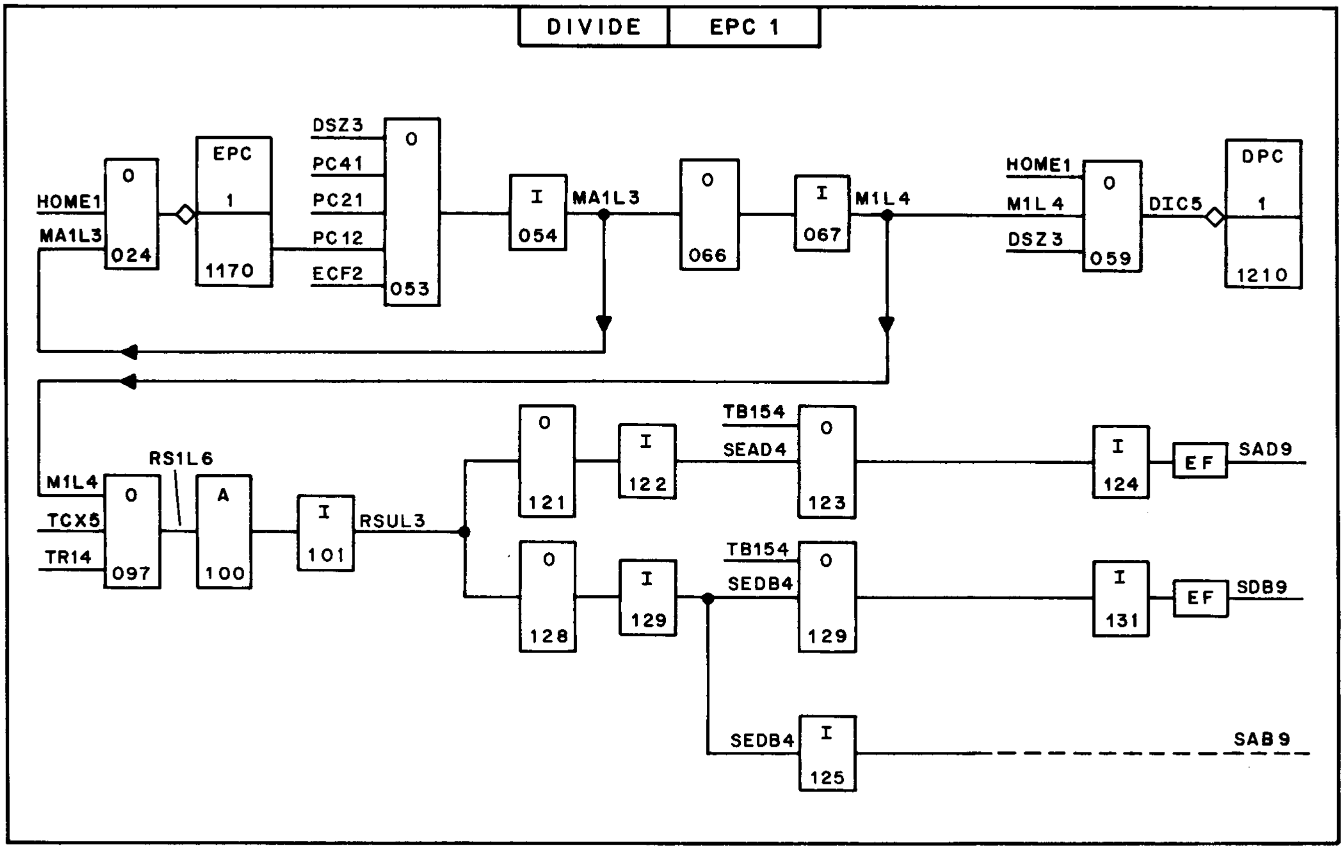


SET FUNCTION FF's. Pressing ÷ Key closes divide reed switch and, by means of an interlocking code bar, also closes Common Function (CF) reed switch. Closing Divide Switch enables an AC gate at the set input of Divide FF. Approximately 6 milliseconds later the Keyboard Delay (EKBD3) pulse, which is initiated by the closing of the CF reed switch, is applied as a + transition signal to the Divide FF set input AC gate, and the transition sets Divide FF. At the same time, closing of CF switch not only initiates EKBD3 signal but also enables an AC gate on the Set input of CF FF. EKBD3 signal is applied 6 milliseconds later to this AC gate, and the transition sets CF FF.

UNCLAMP EPC. CF FF set output (ECF1) provides a + transition that sets Common Function Storage (CFS) FF if CFS is in a reset condition, which in turn sets Decimal Point Storage (DPS) FF. CFS will be reset only if the last operation performed at the keyboard was a number entry. If the number is not decimal aligned by ENTER Key, then the first step of any function is to Decimal Align. However, if the last operation at the keyboard was a function, then the number in R1 is already decimal aligned and CFS is set, therefore CF set cannot set CFS and no setting is placed into DPC. Also, the set output (True) of CF FF is applied through O-016 to I-017, and inverted False, designated ECFD4. Previous to the setting of CF FF, ECF1 was False, inverted True by I-017, and applied to diodes that clamped the EPC FF's to reset, which is EPC Zero. When CF is set, the False output of I-017 (ECFD4) removes the clamping action of the diodes at the EPC FF's, and the next Home time steps EPC to 1.

SET DPC. Multiply FF is reset, thus set output (EMU1) is False, and, inverted to True by I-027, is applied as an enable signal (DEDS3) through the decimal point switch wafers to AC gates at the set inputs of the Decimal (Point) Counter (DPC) FF's. The Decimal Point switch position determines which of the DPC FF AC gates are enabled. In this case, with the Decimal Point switch on 2, DPC8, DPC4, and DPC2 are enabled. (See DPC discussion.)

When DPS sets, EDPS1 + transition is applied at all DPC FF AC gates. Since only DPC8, DPC4 and DPC2 are enabled, only those DPC FF's set. Thus, the setting of DPC represents 14, and two more counts, or advances, are necessary to bring DPC to zero. This is the condition for Decimal Align with the decimal point switch on 2, and the decimal point position designating two places to the right of the decimal point.



DIVIDE - EPC1

The logic action of Decimal Align in Divide function EPC1 is exactly as described in EPC step 1 of multiply, and the same gates are involved. When Decimal Align is completed, MA1L3 at O-024 goes False and the next Home time steps EPC to 2.

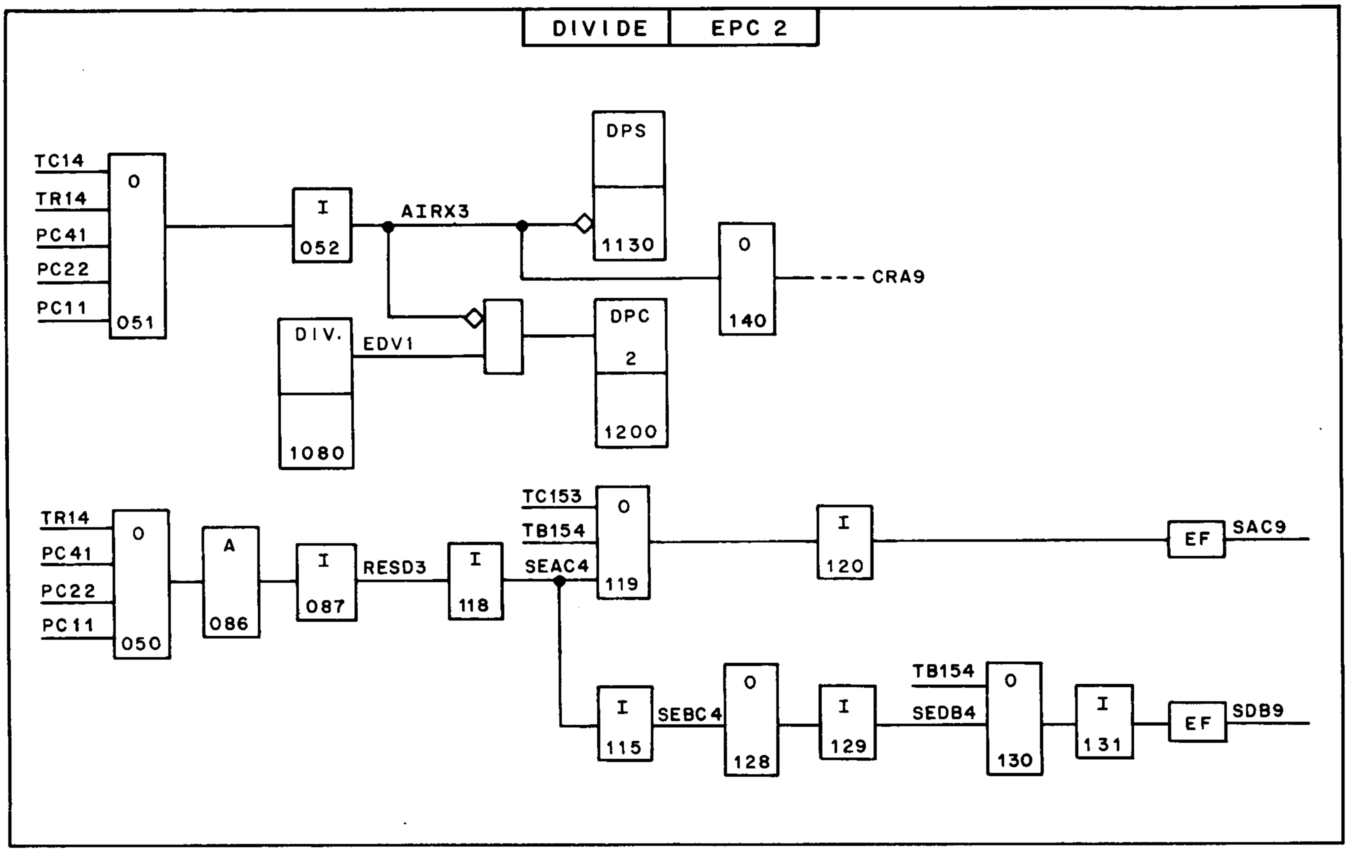
DIVIDE - EPC2

SET DPC TO 2. In Divide function at EPC step 2, DPC is set to a number (2) which represents the 16's complement of the number of digit display columns (13) plus one, or fourteen (14). This is accomplished by O-051 which is enabled by PC11, PC22, and PC41. These inputs will all be False during EPC step 2. When TC14 and TR14 are also False, which will be at C1R1 time, O-051 output will be False. The False output of O-051, inverted True by I-052 (AIRX3), is applied as a + transition to an AC gate at the set input of DPC2 FF. Divide FF set output (EDV1), which is True because Divide is set, is applied as an enable to this AC gate, and DPC2 sets. Since all other DPC FF's are reset at this time, DPC2 FF being set represents DPC set to a count of 2, and it will take 14 more counts, or advances, to bring DPC to zero.

RESET DPS. The False to True output transition of I-052, designated AIRX3, is also applied to reset DPS FF at this time.

COMPARE SIGNS. During EPC2, the sign of the answer is determined by adding the signs of R1 and R2. This is accomplished by inhibiting (blocking) reset of A Counter (CRA9) at the end of C1R1 time. AIRX3 is True during EPC2 and C1R1 time and, applied through O-140, will inhibit CRA9, which would normally occur at the end of C1R1 time. CRA9, if not inhibited, would reset A Counter to zero.

If both signs are +, there is no sign pulse in either C1R1 or C1R2, therefore no change in sign. If both signs are negative, however, there is a sign pulse in C1R1 and C1R2. The blocking of CRA9 leaves A set to 1 by C1R1 sign pulse. Then C1R2 counts "on top" of the 1, and A Counter sets to 2. The next A to B shift places this 2 setting in B Counter. A count of 2 in B Counter during C1 time is used to enable logic gates that reset B to 0 which removes the sign pulse from C1R2 (See Change Sign discussion). Thus, if the signs of R1 are the same, either both + or both -, the sign of C1R2 will be + (no sign pulse in C1R2).



If C1R1 is negative, A Counter sets to 1. Inhibit of CRA9 leaves this 1 in A, and C1R2 counts on top. If C1R2 is +, there is no sign pulse and A remains at 1, and this becomes the sign of C1R2 and R2 sign becomes negative. If C1R1 is +, inhibit of CRA9 leaves A set to 0, (no sign pulse in C1R1) and C1R2 counts on top. If C1R2 is negative (sign pulse in R2) A sets to 1, this becomes the sign of C1R2, and R2 sign is negative. Thus, if signs of R1 and R2 are not the same, the sign of C1R2 will be negative.

SHIFT DOWN R1 TO R0. Since all arithmetical functions of the EC-130 are performed with one of the numbers being in R0 time, the contents of Register 1 (R1) are shifted to R0. This represents a "Shift Down" operation. This is controlled by O-050. PC11, PC22, and PC41 at the input specify EPC step 2, and are False during EPC step 2. TR14 will be False during R1 time, and the output of O-050 will be False during R1 time. False output of O-050 is applied through A-086 to I-087 and inverted True, designated RESD3. RESD3 is inverted False by I-118 (SEAC4) and applied to enable O-119. The other inputs to O-119 are TB154 and TC153. TC153 is False during all C times except C15, thus is False from C1 through C14 time. Therefore, the output of O-119 will be False each B15 time from C1 through C14 as long as SEAC4 is False. False output of O-119, inverted True by I-120, is applied through an emitter-follower as SAC9 to the counter circuits to initiate an A to C shift of data every B15 time at R1 time during C1 through C14 time.

False output of I-118, inverted True by I-115, designated SEBC4, is also applied through O-128 to I-129, and inverted False. The output of I-129 is designated SEDB4 and enables O-130. The other input to O-130 is TB154, which means there will be a False output from O-130 every B15 time as long as SEDB4 is False. False output of O-130, inverted True by I-131, is applied through an emitter-follower as SDB9 to the counter circuits to initiate a D to B shift each B15 time at R1 time during C1 through C14 time.

The result of the A to C shift is to move R1 data into R0 time, which puts significant data into R0 for use in the arithmetical process. The D to B shift places zeros in R1 time, thus effectively clearing R1 for later arithmetical use.

The logic action in EPC step 2 takes place during one pass of data through the counters. At the next Home time at gate O-024, EPC steps to 3.

DIVIDE - EPC3

The flow chart for Divide function states that R0 is subtracted from R1 during EPC step 3. This is done by "Complementary addition". The complement of R0 data is derived by counting R0 into D Counter, digit by digit, then transferring this complement to A Counter so that R1 data can be added to this complemented R0 data.

COMPLEMENTARY ADD. The inputs to O-045 are False during EPC step 3 when Divide FF is set. False output of O-045 is applied through A-046 to I-047 and inverted True, designated MSDS3. MSDS3 is applied through O-069 to I-070 and inverted False, designated MSU4. MSU4 is applied to enable O-071 at R0 (TR04) time, and from C2 through C15 time in a divide function (TCX5) the output of O-071 is False, and inverted True by I-072 is designated AIRS3.

AIRS3 is applied through O-132 to I-133 and inverted False, designated REID4. REID4 is applied to enable O-136. The other input to O-136 is the output of the Read amplifier (XRDL4), which is negative (False) pulses representing data from the Delay Line. As long as O-136 is enabled by REID4 False, XRDL4 will cause pulsed False outputs from O-136. These pulses, inverted True by I-137, designated AIDS3, are applied through O-400 to I-138, double inverted by I-138 and I-139, ending up True, and applied through an emitter-follower as CID9 to D Counter. D Counter advances by one for each pulse. Since D Counter is a "down" counter, each increment pulse (CID9) counts down the delay line R0 pulses from a D Counter setting representing 10, thus taking the 10's complement of the R0 data.

SHIFT D TO A. The shift of R0 data to A Counter from D Counter (D to A) is controlled by O-146. The inputs to O-146 specify that when MSU4 is False; TR04 is False; at any time other than C0 or C1 time (TCX5); when TB154 goes False the output of O-146 goes False. False output of O-146, inverted True by I-147, is applied through an emitter-follower as SDA9 to the counter circuits to shift D Counter data (Complemented R0 data) to A Counter. This means that at R0B15 time for all C times except C0 and C1 there will be a data shift D to A which will place complemented R0 data into A Counter just before R1 time.

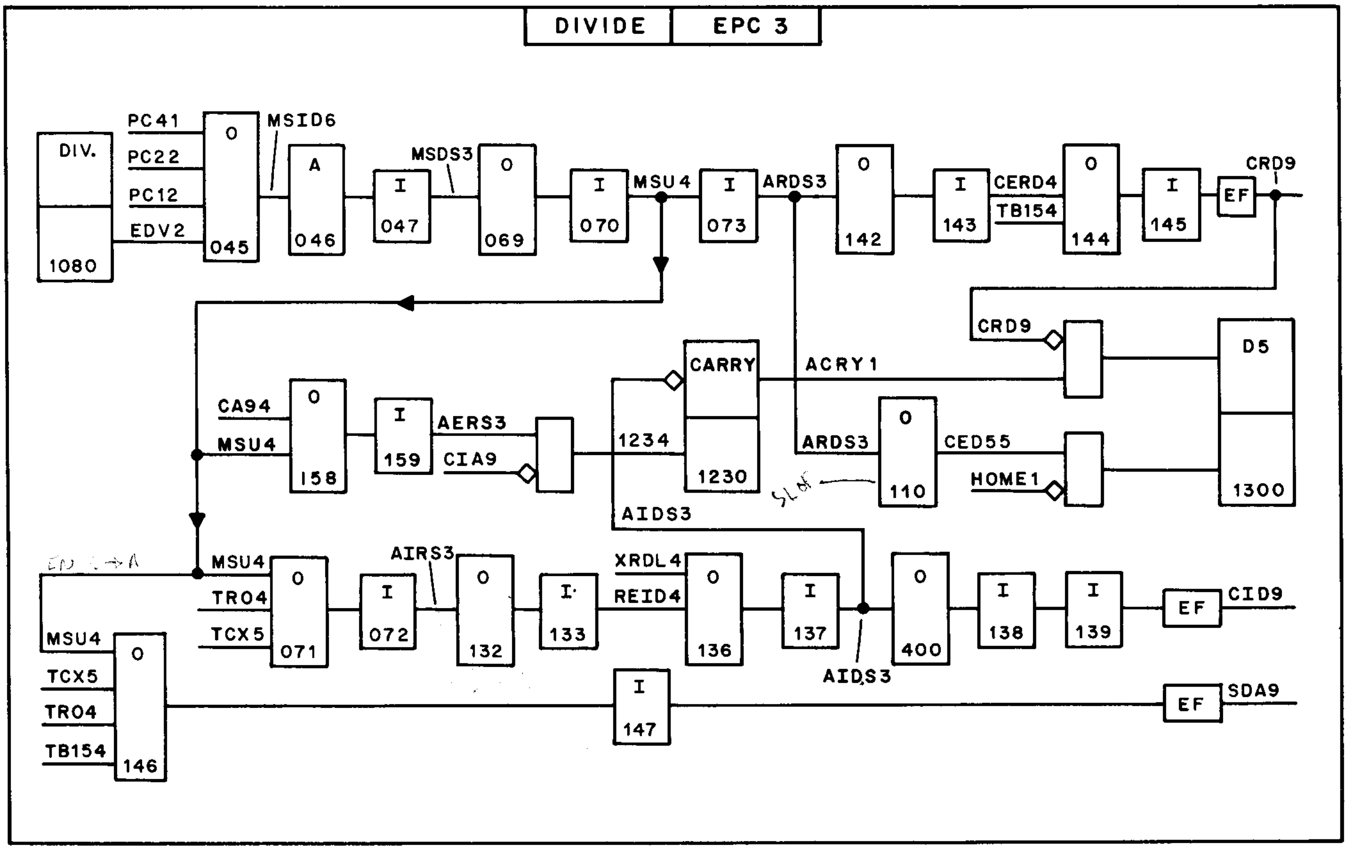
It is important to remember that the R0 data is counted into A Counter at the same time as the R0 data is counted into D Counter. Since the A to B shift is not inhibited by the D to A data shift, the R0 data is shifted unchanged into B Counter at the same time that the complemented R0 data is shifted from D to A. This preserves the R0 data in the data sequence.

SET CARRY. The first pulse from the Read Amp (XRDL4) through O-136, inverted True by I-137, designated AIDS3, sets Carry FF. The set output (True) of Carry FF (ACRY1) is applied to enable an AC gate at the set input of D5 Counter FF. MSU4, inverted True by I-073, designated ARDS3, is applied through O-142 to I-143 and inverted False, designated CERD4. CERD4 is applied to enable O-144. The other input to O-144 is TB154, which means that there will be a False output from O-144 each B15 time when O-144 is enabled by CERD4. False output of O-144, inverted True by I-145, is applied as CRD9 to the AC gate at D5 set input that is enabled by Carry FF set output (ACRY1). The CRD9 transition from I-145 will set D5 and reset all other D FF's each B15 time as long as Carry FF is set. If the "Read in D" starts with D5 set and all other D FF's reset, the count starts from D setting of 9 instead of 10 thus showing the presence of a borrow for the previous column complementing action, which means taking the 9's complement.

RESET CARRY. However, if A Counter goes past 9 during addition of R0 (complemented) to R1, then the borrow will be canceled. This is controlled by O-158 enabled by MSU4 from I-070. If A reaches 9 during a subtract (in Divide), then O-158 has both inputs False, and the output will be False. False output of O-158, inverted True by I-159, designated AERS3, is applied to enable an AC gate at the reset input of Carry FF. The next increment A transition (CIA9), which would at the same time count A to 10, resets Carry. When Carry is reset, D5 set input AC gate is not enabled, D5 as well as all other D FF's starts the new "Read in D" from a reset condition, and the new "Read in D" starts from a setting of 0 (10) in D Counter, which means taking 10's complement, and also indicates that the borrow has been cancelled.

An AC gate at the reset input of D5 Counter is enabled through O-110 by ARDS3 being True (I-073). At the beginning of Home time, the HOME1 at this AC gate resets D5 to ensure that D Counter starts from 0 at the next register sequence of "Read in D" even if Carry FF is still set. In other words, D Counter is definitely set to zero at Home time.

Subtract R0 from R1 is completed in one pass of the data through the counters, and HOME1 at O-024 steps EPC to 4.



COF Resets in 4 + 5

DIVIDE - EPC4

DPC ZERO? In EPC4 of divide, if DPC is zero and DPS is reset, then DPC is set to the 16's complement of the chosen decimal position, in this case to 14. If DPC is zero, all inputs to O-057 are False, and the output is False. False output of O-057, inverted True by I-058, designated DSZ3, is applied to enable an AC gate at the set input of DPS FF. EDV1, applied through O-009 to I-010 and inverted False, is applied to enable O-011. When EPC steps to 4, PC42 input to O-011 goes False, and the output goes False. False output of O-011, inverted True by I-012, designated P4SD3, is applied as a + transition signal to the AC gate at DPS set input, and sets DPS.

SET DPC. AC gates at the set inputs of DPC FF's are enabled through the Decimal Point switch wafers by MULT FF set output (EMU1) inverted True by I-027, designated DEDS3. Set output of DPS FF (EDPS1) is applied to all DPC AC gates as a transition signal. However, only those DPC FF's enabled by the Decimal Point switch wafers will set, in this case DPC8, DPC4, and DPC2. This represents a preset condition of 14 and two more counts, or increments, will bring DPC to zero. This corresponds to the Decimal Point position of 2 with two columns available to the right of the decimal point.

COF SET? If DSZ3 is not True, however, DPS does not set. The logic then is to check whether Carry Overflow (COF) FF is set. COF will set when an unsuccessful subtract (complementary add) in EPC3 or EPC4 has left Carry FF set at Home time. If Carry is set at Home, the set output (ACRY1) enables an AC gate at COF FF set input. HOME1 then provides a transition through O-160 at this gate which sets COF, which in turn permits EPC to step to 5 through O-043, which removes MIAD3 (True) inhibit on O-024. If COF is set, ACOF1 input at O-043 will be True, the output of O-043 True and, inverted by I-044, the signal MIAD3 will be False. MIAD3 (False) at O-024 at EPC1 FF will permit HOME1 to step EPC to 5 and no further logic action in EPC4 will occur.

Assume in EPC step 3 that the "subtract of R0 from R1" is unsucessful, which will always occur when EPC steps from 2 to 3 because R1 has been cleared in EPC step 2 and contains no data. The unsuccessful subtract (overdraft) leaves Carry set at Home time, which sets COF. COF being set when EPC steps to 4 means no logic action in step 4, and the next Home time steps EPC to 5. In EPC5, R0 is directly added into R1 with no complementing, thus the overdraft is corrected and R1 returns to whatever data setting it was before the overdraft.

Carry o'flow sets with unsuccessful sub.

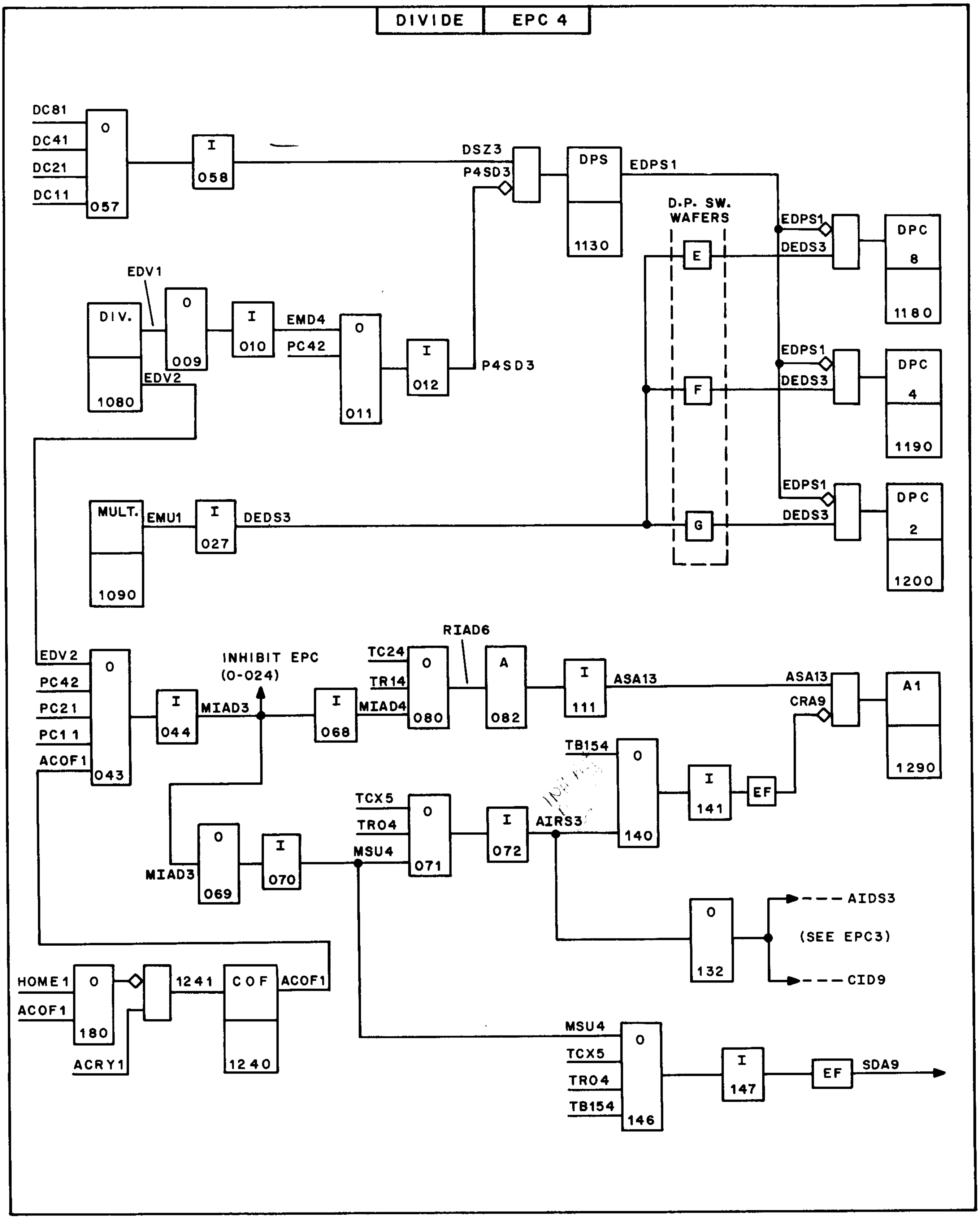
SUBTRACT R0 FROM R1. Now assume that, due to a previous step 6 in the subtract loop, R1 contains enough data so that R0 (complemented) added to R1 does not leave Carry set, which in turn means that COF does not set. Now, in EPC step 4, further subtracts can take place. The first subtract in EPC4 will add 1 to R2 even if unsuccessful, so effectively, the first subtract in EPC3 results in an Add 1 to R2 in EPC4. EPC will stay on step 4 as long as COF does not become set in a subtract cycle and the last (unsuccessful) subtract that results in COF set will still add 1 to R2, which takes care of a possible successful subtract in EPC3. In other words, the subtract in EPC3 will add 1 to R2 in EPC step 4.

EPC4 subtract cycle is controlled by O-043. If COF is not set by HOME1, ACOF1 is False and enables O-043. The other inputs to O-043 specify EPC step 4 and Divide function, and will be False. False output of O-043 acting as a -AND is inverted True by I-044, designated MIAD3. MIAD3 is applied to inhibit O-024, which keeps EPC from stepping off 4 when MIAD3 is True.

MIAD3 True is applied through O-069 to I-070 and inverted False, designated MSU4. MSU4 enables O-071 and O-146, which control "Read in D" and Shift D to A exactly as in EPC step 3. This is a part of subtract (Complementary Add).

ADD 1 TO LSD OF R2. MIAD3 is also applied to I-068, inverted False (MIAD4), and applied to enable O-080. The other inputs to O-080 specify False at C2R1 time. During C2R1 time the False output of O-080, designated RIAD6, is applied through A-082 to I-111, inverted True, designated ASA13, and applied to enable an AC gate at set input of A1 Counter FF. At the end of C2R1 time, CRA9 (True) is developed and, applied to the AC gate, sets A1 FF and resets all other A FF's. A Counter, then, starts the next data count (C2R2) from a setting of 1, or 1 has been added to C2R2 (LSD of R2).

Due to MIAD3 (True) at O-024, EPC remains on step 4 until an unsuccessful subtract leaves Carry FF set at Home time which sets COF. COF set makes ACOF1 True at O-043. ACOF1 True through O-043 is inverted False by I-044 (MIAD3). MIAD3 False at O-024 enables the next HOME1 to step EPC to 5, and logic action in EPC step 4 is complete.


DIVIDE
EPC 4
DC81
DC41
DC21
DC11
O
057
I
058
DSZ3
P4SD3
DPS
1130
EDPS1
D.P. SW. WAFERS
E
F
G
EDPS1
DEDS3
DPC 8
1180
DPC 4
1190
DPC 2
1200
EDV1
DIV.
1080
009
EDV2
I
010
EMD4
PC42
011
012
P4SD3
MULT.
1090
EMU1
027
DEDS3
EDV2
PC42
PC21
PC11
ACOF1
043
044
MIAD3
INHIBIT EPC (0-024)
068
MIAD4
TC24
TR14
080
RIAD6
A
082
111
ASA13
ASA13
CRA9
A1
1290
TB154
140
141
EF
TCX5
TR04
MSU4
071
072
AIRS3
MIAD3
069
070
132
AIDS3
(SEE EPC3)
CID9
HOME1
ACOF1
180
ACRY1
1241
COF
1240
ACOF1
MSU4
TCX5
TR04
TB154
146
147
EF
SDA9

DIVIDE - EPC5

In EPC step 5, the overdraft that occurred in EPC step 4 is cleared by adding R0 (not complemented) to R1, which brings R1 back to what it was before the subtract which produced the overdraft.

DPC ZERO? If DPC is not zero, meaning that the Divide function arithmetic is not complete, DSZ3 will be False at O-039. The other inputs to O-039 specify EPC step 5 and Divide function (EDV2), and will be False. When all inputs to O-039 are False the output is False and inverted True by I-040, designated MAID3.

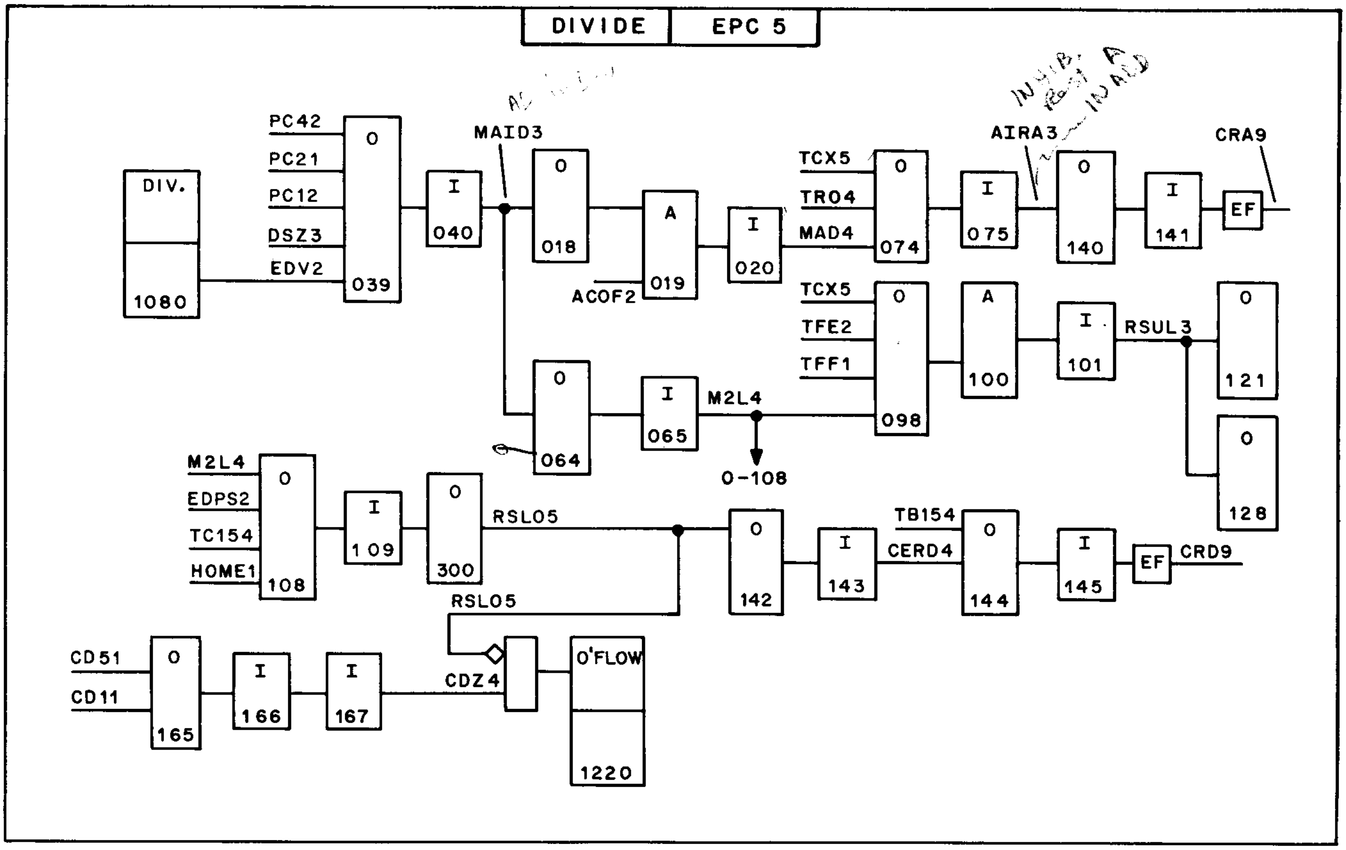
ADD R0 TO R1. MAID3 is applied through O-018 to A-019. ACOF2 will be True at A-019 because the Home time that stepped EPC to 5 also reset COF. When both inputs to A-019 are True, the output is True and, inverted False by I-020, is designated MAD4.

MAD4 enables O-074. The other inputs to O-074 specify R0 time (TRO4), and C2 through C15 time (TCX5), and will be False. False output from O-074, inverted True by I-075, designated AIRA3, is applied through O-140 to I-141, and inverted False. The output of I-141 resets A Counter when True. When I-141 output is False, reset of A Counter is blocked at the end of each R0 time; R0 data setting remains in A Counter; and R1 data counts in "on top", thus adding R0 data to R1 data.

False. The output of I-141 resets A Counter when True. When I-141 output is False, reset of A Counter is blocked at the end of each R0 time; R0 data setting remains in A Counter; and R1 data counts in "on top", thus adding R0 data to R1 data.

SHIFT R2 LEFT. To control shifts of R2 data left, MAID3 from I-040 is applied through O-064 to I-065, inverted False, designated M2L4, and enables O-098. TCX5 at O-098 specifies C2 through C15 time. TFF1 and TFE2 at O-098 specifies R2 time. The output of O-098 will be False during R2 time from C2 through C15 time when M2L4 is False. False output of O-098 is applied through A-100 to I-101 and inverted True, designated RSUL3. RSUL3 is applied through O-121 and O-128 to control A to D and D to B shifts exactly as in EPC step 1 (Decimal Align) except that the shifts are specified for R2 data. The last shift of R2 left at C15 time will leave the MSD of R2 (C15R2) in D Counter where it is available to be shifted into the LSD of R1 (C2R1) at the next R1 shift left in EPC step 6.

TFF1, TFE2, R2



RESET D. The shift of D Counter into R1 (MSD of R2 to LSD of R1) is a part of the arithmetic of the divide problem and will occur until DPC counts down to zero from the setting established in EPC step 2. The first DPC setting in step 2 occurs when AIRX3 goes True at DPC2 FF and at the same time DPS is reset. DPS sets again in EPC4 when the original DPC setting has counted to zero. This signifies that the arithmetic of the problem is completed. When DPC is set again by DPS in EPC step 4 to establish decimal align of the answer, DPS remains set. Now, during R2 shift left of decimal align of the answer, it is not desired to leave R2 data in D at C15 time for later placement into R1 because the arithmetic is complete. Therefore, DPS being set is used to establish a specific reset of D Counter to zero at C15 time. Also, if there is data in D Counter, which would be part of the answer, Overflow FF is set to designate the overflow condition.

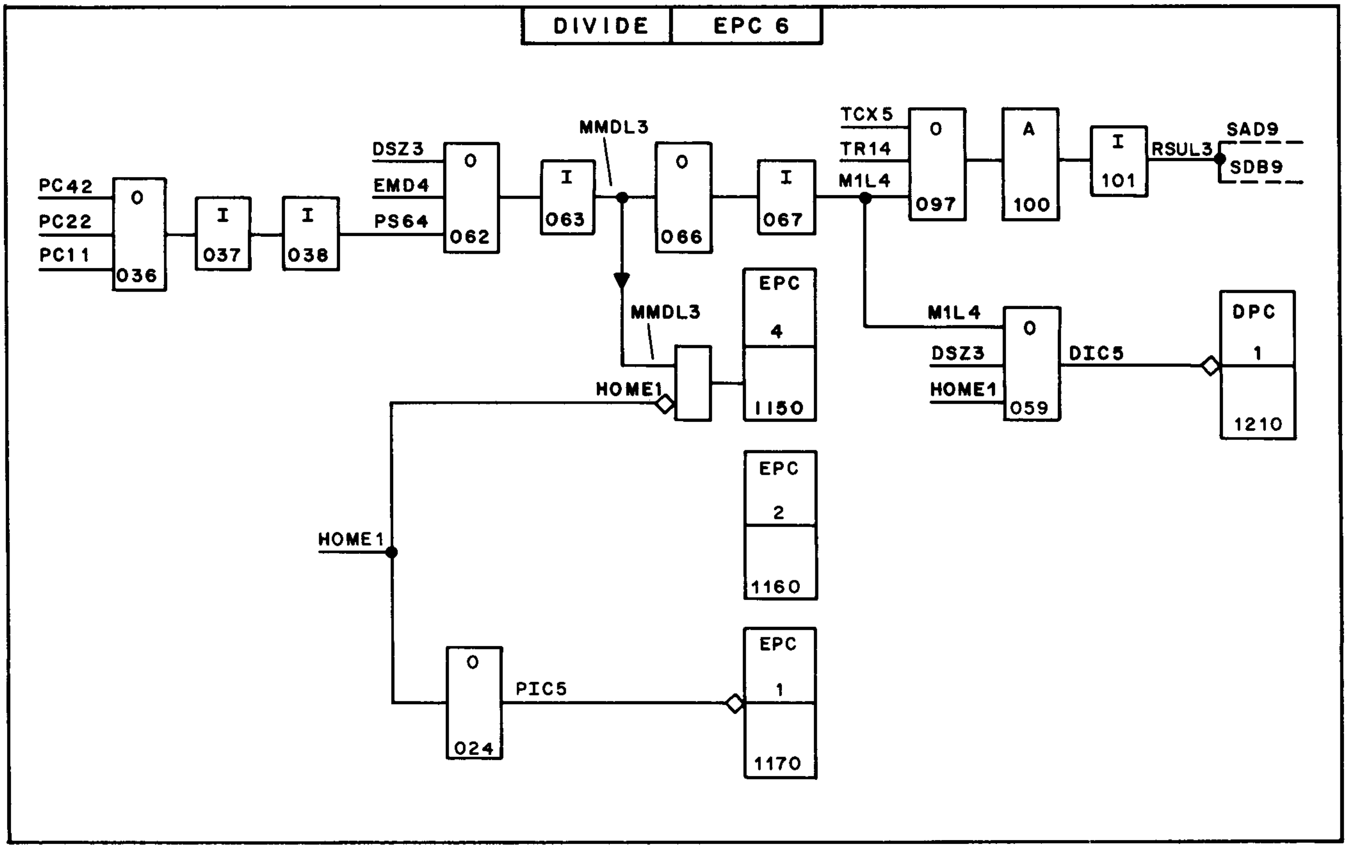
M2L4 is applied as an enable signal to O-108. The other inputs to O-108 are HOME1, EDPS2, and TC154. This means that during a shift 2 left, at C15 time if DPS is set, TC154 going False will cause a False output from O-108. O-108 False, inverted True by I-109, is applied through O-300 (RSLO5) and O-142 to I-143, inverted False, designated CERD4, and enables O-144. When TB154 goes False, which will be each B15 time, O-144 output goes False. O-144 False is inverted True by I-145 and is applied through an emitter-follower as CRD9 to D Counter, and resets all D FF's.

SET OVERFLOW. The overflow condition is qualified by whether there is data in D Counter at the time RSLO5 goes True. At gate O-165, either CD51 or CD11 will be True if there is data in D. True output of O-165, double inverted by I-166 and I-167, enables an AC gate (1222) at set input of Overflow FF. When RSLO5 goes True, the transition sets Overflow FF, which enables keyboard lock-up and Overflow light.

Logic action of EPC step 5 takes one pass of data through the counters, and the next HOME1 at O-024 will step EPC to 6.

DIVIDE - EPC6

The logic of EPC step 6 is a part of the arithmetic of the problem. Logic function is to Shift R1 left, count DPC up by one, and step EPC 6 to 3 instead of 6 to 7 if arithmetic is not completed. DSZ3 (DPC zero) at O-062 is the determining logic condition that designates whether arithmetic is complete.



DSZ3 at O-062 will be False if DPC is not zero, which signifies that arithmetic is not completed. EMD4 at O-062 specifies, in this case, Divide function, and PS64 specifies EPC step 6. False output of O-062 is inverted True by I-063, designated MMDL3.

SHIFT R1 LEFT. MMDL3, applied through O-066 to I-067 and inverted False, designated M1L4, enables O-097. The output of O-097 is applied through A-100 to I-101 and, inverted True (RSUL3), enables A to D and D to B shifts of R1 left exactly as in EPC step 1, Decimal Align. As a part of shift R1 left, data which was left in D Counter by the previous shift R2 left is placed in the LSD of R1 (C2R1) by the first D to B shift in the shift of R1 left.

Wrong

S/B DPC

COUNT DPC UP 1. M1L4 is also applied to enable O-059, which permits HOME1 to step DPC by 1 each Home time as long as (D Counter) is not zero (DSZ3 False). This means that DPC will count up by one for each shift of R1 one column left until DPC reaches zero (DSZ3 True).

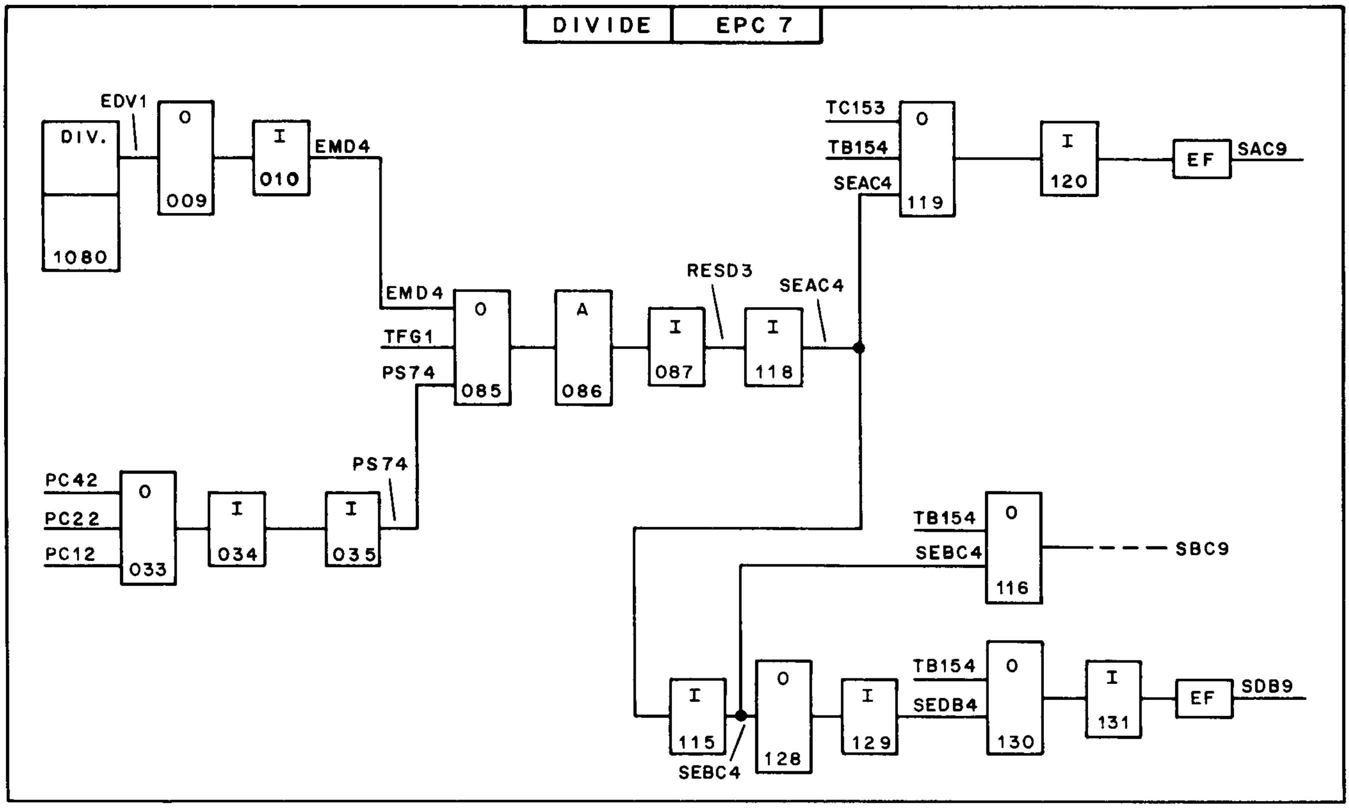
STEP EPC TO 3. MMDL3 (True) is also applied to enable an AC gate at reset input of EPC4 FF. The action of this gate is covered in Entry Phase Counter discussion and the result of MMDL3 enabling this gate is that EPC steps from 6 to 3 instead of 6 to 7.

STEP EPC TO 7. If DSZ3 is True (DPC Zero) at O-062, which indicates arithmetic is complete, O-062 output is True and MMDL3 will be False. MMDL3 False inhibits any R1 shifts left; inhibits count DPC up by 1; and, inhibits step EPC 6 to 3. The result, then, is that no logic action occurs in EPC step 6 and the next Home time at O-024 steps EPC 6 to 7. This is designated on the Divide Flow Chart at BYPASS on EPC step 6.

DIVIDE - EPC7

EPC step 7 indicates that the answer is complete and decimal aligned in R2. Since R1 is the answer register, R2 must be shifted to R1, which is a shift down and is accomplished by A to C and D to B shifts at specified times.

SHIFT DOWN. Shift down in a Multiply or Divide function is controlled by O-085. EMD4 specifies, in this case, Divide function; PS74 specifies EPC step 7; and TFG1 specifies R1 through R4 time. False output of O-085 is applied through A-086 to I-087 and inverted True, designated RESD3. RESD3, inverted False by I-118 is designated SEAC4. SEAC4 enables O-119 which controls A to C exactly as in EPC step 2. SEAC4, inverted True by I-115, designated SEBC4, inhibits O-116, which inhibits B to C shift. SEBC4 (True) is applied



through O-128 to I-129 and inverted False, designated SEDB4. SEDB4 enables O-130, which controls D to B exactly as in EPC step 2.

After one pass of data through the counters R1 through R4 have been shifted down. This places R2 data in R1 for display.

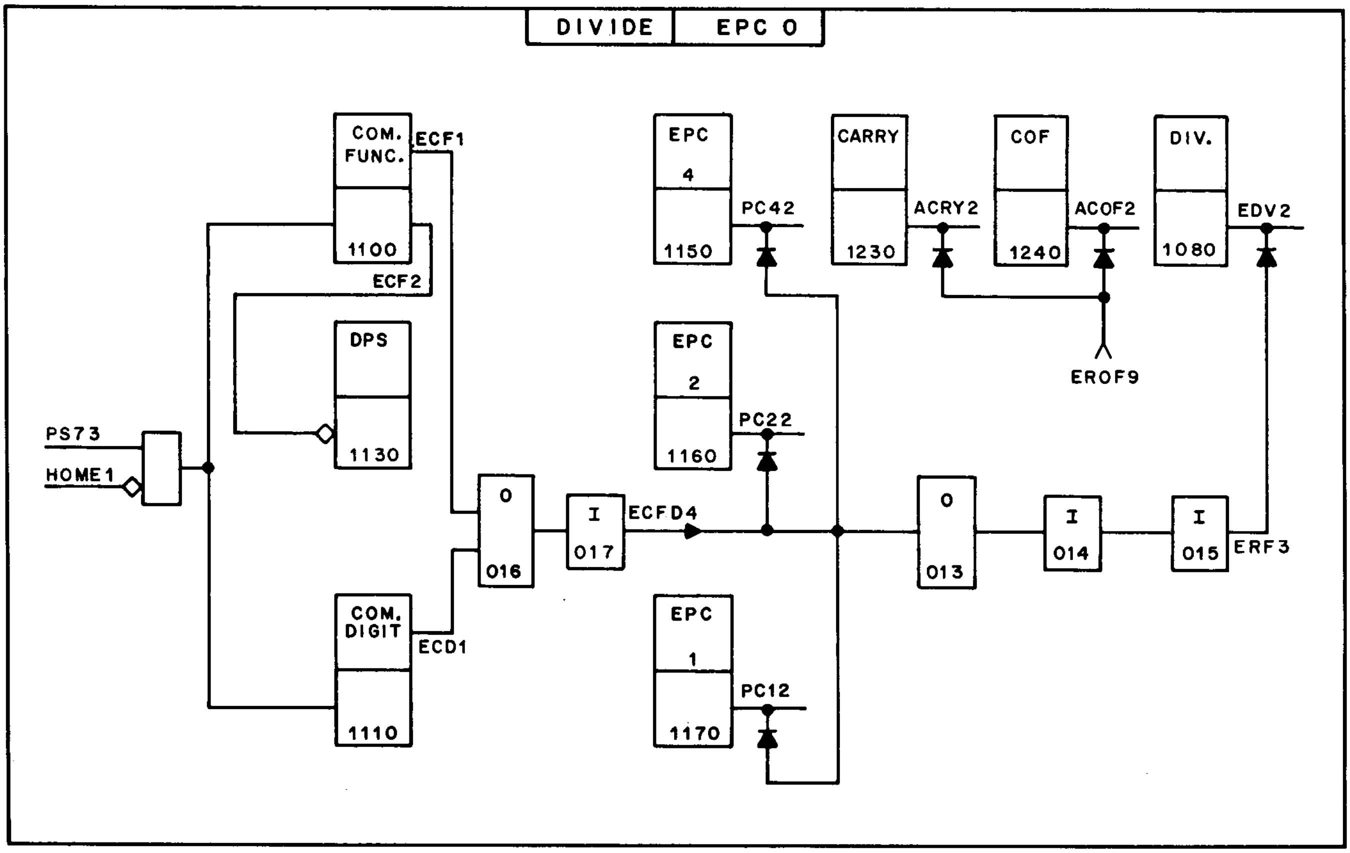
PS73 from I-034 is applied to enable an AC gate which is common to the reset inputs of both CF and CD. The next HOME1, which is the end of EPC7, at this AC gate resets CF (CD is still reset). This same HOME1 at O-024 steps EPC to zero, which makes PSZ3 True.

DIVIDE - EPC0

CLAMP EPC TO 0. Reset of CF (ECF2 True) at the end of EPC step 7 resets DPS. ECF1 going False when CF resets makes both inputs of O-016 False since CD is reset (ECD1 False, False output of O-016 is inverted True by I-017, designated ECFD4. ECFD4 (True) clamps EPC to 0.

RESET FUNCTION FF's. The False to True output transition of I-017 (ECFD4) is applied through O-013 to I-014, double inverted by I-014 and I-015, ending up as a False to True transition at I-015 output, designated ERF3. ERF3 True is applied to reset any function FF's that are set, in this case, Divide FF.

ENABLE DISPLAY. PSZ3 going True at A-225 in the Display logic when EPC steps to zero enables Display, and Divide function is complete.



5. NUMBER ENTRY

In accounting, an entry is considered to be the recording of a complete number in proper decimal alignment. A number is one or more digits. A digit is a part of a number. In the EC-130, a number is placed in the machine digit-by-digit, which is designated "Digit Selection", and then decimal aligned as a part of a function or by ENTER key, which is designated "Number Entry". For clarity, these operations will be discussed separately. (See Flow Charts Figures 2-34 and 2-35.)

a. DIGIT SELECTION. Each digit of a number is placed in the machine by pressing a numeral key, numbered one (1) through nine (9). Each key actuates one or more digit code bars, numbered 1 through 5, and also actuates Common Digit (CD) code bar. CD code bar movement is common to all numeral keys. (See Keyboard Function discussion.) The code bars, in turn, actuate reed switches. When the reed switches are closed they act as enable inputs to AC gates on respectively numbered D Counter FF's. (See Figure 2-33.) Enabled D FF's are then triggered to set condition by a logic signal (ME1L3), and the setting of D FF is placed in the data sequence at C2R1 time. Each digit as selected is placed in the same specific time, C2R1. When the next digit is selected, the previous digit, or digits, are shifted left so that C2R1 time becomes available for the new digit.

UNCLAMP EPC

All numeral keys (0 through 9) move CD code bar to operate position, which closes CD reed switch. When CD reed switch closes, KBD is initiated and CD FF set input AC gate is enabled. Approximately 6 ms later, EKBD3 sets CD FF which makes ECD1 go False to True at O-016. When either input of O-016 goes True, output goes True, and makes ECFD4 go False, which removes the clamp on the EPC FF's exactly as in Add and Subtract functions.

There is no logic action in EPC step 1 of Digit Selection because DPS does not become set therefore DPC remains on zero. The next HOME1 time steps EPC to 6 exactly as in Add and Subtract functions.

In EPC step 6, the logic actions diverge depending on whether there is data in R1. If this is the first Digit Selection after the machine has been cleared, there is no data present in R1, no logic action occurs in EPC step 6, and the next HOME1 time steps EPC to 7. However, if the Digit Selection occurs after a function, which includes use of ENTER key, then logic action occurs in EPC step 6 which shifts up data in R1 so that the new digits may be entered.

EPC STEP 6 - SHIFT UP

Shift Up is controlled by O-099 (Figure 2-33). When a digit key sets CD FF, ECD2 goes False. If a number has been previously entered, or a function has been performed, CFS FF will be set and ECFS2 will be False. PS64 specifies EPC step 6, and TFG1 specifies R1 through R4. When all inputs to O-099 are False, RSUL3 becomes True and enables A to D and D to B shifts that result in Registers 1 through 4 shifting up. The A to D shift for R4 leaves R4 data in D Counter. This would be placed in the next R1 time if D Counter were not reset to zero by other means. Reset D (CRA9 True) is controlled by O-102. ECD2, ECFS2 and PS64 will be False as explained above, and TRO4 specifies R0 time. At R0 time, then, O-102 output is False and CRA9 becomes True at R0 B15 time and is applied to reset D Counter to zero. Then, the D to B shift in R1 time places zeroes in R1, which effectively clears R1 for the entering of digits. The next HOME1 time steps EPC to 7.

EPC STEP 7

The logic action in EPC step 7 of Digit Selection is the same whether it occurs during an initial Digit Selection, or a Digit Selection after a function or Number Entry. O-060 is enabled by ECD2, which will be False because CD FF is set. PS74 will be False during EPC step 7. DBDE and DBSL3 will be False except under special circumstances which will be discussed separately. When EPC steps 6 to 7, the False output of O-060 is applied to I-061 and inverted True, designated ME1L3. ME1L3 False to True transition at D FF AC gates sets those FF's enabled by digit reed switches being closed. D Counter setting then represents, in binary form, the numeral key that was pressed.

ME1L3 through O-066 is inverted False by I-067, designated M1L4, and applied to enable O-097. TCX5 at O-097 will be False from C2 through C14 time, and TR14 will be False for R1 time. The output of O-097, then, is False for R1 time from C2 through C14 time. False output of O-097 is applied through A-100 to I-101 and inverted True, designated RSUL3. RSUL3, when True, enables A to D and D to B shifts at R1B15 time for all C times (C2 through C14) which moves all data one column left.

The first A to D shift moves C2R1 data from the data sequence into D Counter to be held until C3R1 time, when it will be placed back into the data sequence. At the same time, D Counter data setting, which represents the numeral entered, is placed in B Counter by the D to B shift that occurred with the A to D shift. This places the entered digit in C2R1 time. The net result of the

D COUNTER TRUTH TABLE

	(D1)	(D2)	(D3)	(D4)	(D5)
(10)	0	0	0	0	0
9	0	0	0	0	1
8	0	0	0	1	1
7	0	0	1	1	1
6	0	1	1	1	1
5	1	1	1	1	1
4	1	1	1	1	0
3	1	1	1	0	0
2	1	1	0	0	0
1	1	0	0	0	0
0	0	0	0	0	0

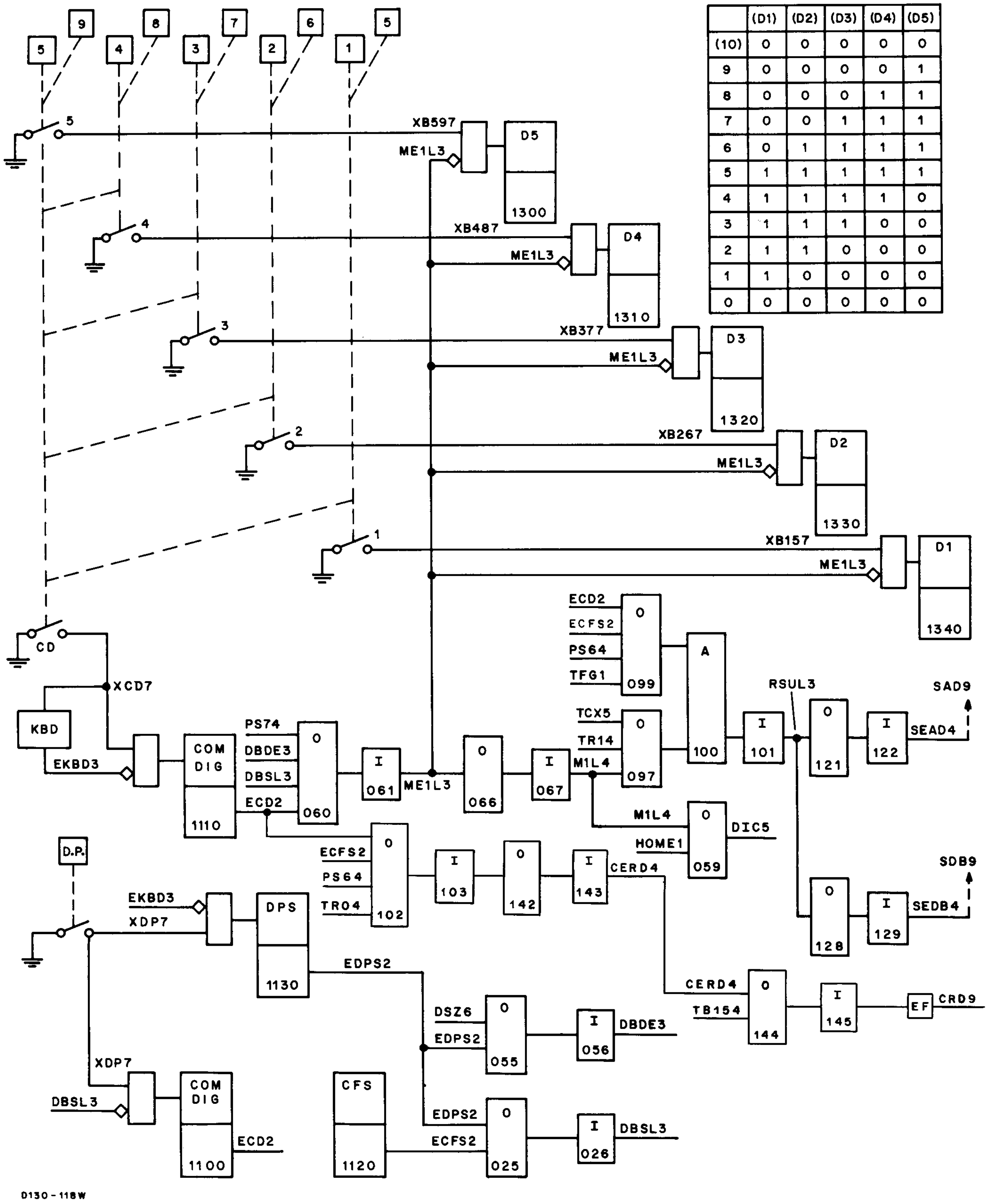


Figure 2-33. Digit Selection Logic

Attempted entry of more than 13 digits will cause an Overflow condition which will result in keyboard lock-up and OVERFLOW LOCK key lighting up. (See Keyboard discussion.)

A to D and D to B shifts is to move all data, even if zeros, one column left and place D Counter data into the vacant C2R1 time. This action will occur for each entered digit, starting with the first digit entered, until the 13 possible digits have been entered.

b. DECIMAL INTERLOCK. Decimal Interlock is special logic that prevents the entering of more digits than there are column spaces to the right of the decimal point position. Assume the Decimal Point switch is on 2, there are two digit display columns to the right of the decimal point. If a three digit decimal number such as .153 is now entered, the machine accepts only the 15 and does not enter the 3. The Decimal Interlock logic is initiated by the Decimal Point Key. Any digits entered without pressing Decimal Point Key are treated as a whole number, and will be placed to the left of the decimal point.

Pressing DECIMAL POINT Key (Figure 2-33) closes D.P. reed switch and also initiates KBD. Approximately 6 ms later, EKBD3 at the enabled AC gate on DPS FF sets DPS. When DPS sets, DPC becomes set to a number that corresponds to the 16's complement of the D.P. position, exactly as in Decimal Align but for a different logic action, which is as follows.

When DPC is set to any number other than zero, DSZ6 is True at O-055. The other input to O-055 is EDPS2, which is False when DPS is set, and DPS became set by action of D.P. Key. When either input to O-055 is True, the output is True, and is inverted to False by I-056, designated DBDE3. DBDE3 False enables O-060, which controls Entry Shift Left logic. Each time a digit is entered there is a column shift left as explained in Number Entry discussion.

Assume DPC becomes set to 14 because D.P. switch is on 2. As long as O-060 is enabled by DBDE3 being False, there can be a shift left for each digit entry. Each digit being entered takes one word time to complete, and at the end of each word time, HOME1 at O-059 counts DPC up by 1. When DPC is counted up to zero, which will be Two Entry shifts left, DSZ6 goes False and both inputs to O-055 are False since DPS is set and EDPS2 is False. When both inputs to O-055 are False, O-055 acts as a -AND and the output goes False, which makes DBDE3 True. DBDE3 True at O-060 inhibits any further shifts left, therefore no more digits can be entered.

c. DECIMAL NUMBER ENTRY. When entering a number that contains only decimals, which means DECIMAL POINT Key is the first key pressed, special logic operations occur to ensure that a shift up clears R1 for the number-entry portion of the operation.

The special logic is controlled by the development of DBSL3 True by I-026. (See Figure 2-33.) If both inputs to O-025, which controls I-026, are False, the output of O-025 is False, and DBSL3 is True. DBSL3 True at O-060 inhibits the usual shifts left that occur on digit entry.

Pressing DECIMAL POINT Key as the initial step in the entering of a decimal number enables AC gates at set input of DPS FF and CD FF, and initiates KBD. 6 ms later EKBD3 sets DPS, which makes EDPS2 False at O-025. CFS is set at this time, therefore, both inputs to O-025 are False, and DBSL3 goes True at the time DPS sets. False to True transition of DBSL3 sets CD FF at an AC gate enabled by D.P. reed switch, when closed.

Set of CD FF makes ECD2 False at O-099. ECFS2 is False because CFS is set. When EPC cycles to step 6, PS64 is False. TFG1 will be False from R1 through R4 time. False from O-099 is applied through A-100 to I-101 and inverted True, designated RSUL3. RSUL3 controls A to D and D to B shifts exactly as discussed under Digit Entry.

The net result, then, of pressing DECIMAL POINT Key as the initial part of a decimal number entry is to cause a shift up of R1 through R4, which effectively clears R1 and digits may now be entered.

Upon the completion of Shift Up in EPC step 6, HOME1 at O-024 steps EPC to 7 and then to EPC0. When EPC goes to EPC step 7, PS73 (True) enables an AC gate common to reset inputs CF and CD FF's. The next HOME1 after EPC7 at this gate resets CD FF, which was set by DBSL3, and at the same time steps EPC to 0. Now, when any numeral key is pressed, the normal number entry operation provides for the insertion of a digit in C2R1 as discussed under Number Entry.

Note that DPS FF remains set after a decimal number entry. This means that after entering the digits of the decimal number, DPS cannot be set for a Decimal Align in the Enter function. Assume that the decimal position is on 5 and a two digit decimal number such as .25 is entered. When the last digit (5) is entered, DPC, which was set to allow a possible five column spaces for decimal digits when D.P. key was pressed, has only been counted up by two (2) by the entering of the 2 and the 5 and has three (3) possible counts left. Now, when ENTER key is pressed, the remainder of the DPC counts shifts all data three columns left, which places the number in proper relation to the Decimal Point position.

d. NUMBER ENTRY - ENTER KEY. When the digits of a number are in the machine in R1, the number is then decimal aligned. Until the ENTER key is pressed, or a function initiated, there is no decimal point displayed in R1, and the entered digits merely occupy the digit places starting from the right-most digit space (C2R1) on the display.

ENTER-BEGIN

ENTER key moves CF code bar which closes CF reed switch. Closing CF reed switch initiates Keyboard Delay and also enables an AC gate at CF FF. Approximately 6 ms later, CF FF sets and ECF1 goes True. The rest of the logic operations such as unclamping EPC and setting Decimal Point Counter are the same as in Multiply, Divide, Add, and Subtract functions. The next HOME1 time at O-024 after EPC is unclamped steps EPC to 1. (See Enter Flow Chart, Figure 2-35.)

ENTER-EPC1

The logic operations in EPC step 1 are to shift R1 data left by the number of columns specified by DPC setting. The logic operations in EPC step 1 of ENTER (Decimal Align) are exactly the same as in EPC1 of Add, Subtract, Multiply, and Divide. At the next HOME1 time EPC steps from 1 to 6 exactly as in Add and Subtract functions.

However, if there are more whole number digits in the entered number than there are columns available to the left of the Decimal Point, an overflow condition will be indicated by Keyboard lock-up and OVERFLOW LOCK Key lighting up. (See Keyboard Function discussion.)

ENTER-EPC6 and EPC7

No logic action occurs during these EPC steps during ENTER. At the next HOME1 time after EPC7, which steps EPC to 0, CF FF becomes reset and clamps EPC to 0. Display unblanks and Enter function is completed.

e. NUMBER ENTRY - FUNCTION KEYS. After Digit Selection, any digits in R1 are automatically decimal aligned, if not already aligned, during EPC step 1 of every function. This will be discussed, as applicable, during EPC step 1 of each function.

6. REPEAT

Repeat function is a means of duplicating R1 data in R2 without the necessity of reentering the same digits.

REPEAT BEGIN

Pressing REPEAT Key (See Figure 2-36) closes Repeat reed switch and, by means of CF code bar action, also closes CF reed switch. Closing Repeat reed switch enables an AC gate on Repeat FF set input. 6 ms later EKBD3 at this gate sets Repeat FF. Closing CF reed switch initiates KBD, unclamps EPC, and sets DPC exactly as in Add and Subtract functions previously discussed. (See Repeat Flow Chart, Figure 2-37.)

REPEAT - EPC1

As in Add and Subtract functions and with exactly the same logic action, display is inhibited, R1 is decimal aligned if not already aligned, and EPC steps from 1 to 6.

REPEAT - EPC6

The logic action is EPC step 6 is to duplicate R1 data in R2 time and, at the same time Shift Up R2 through R4 to clear R2 for R1 data insertion. Shift up is accomplished by A to D and D to B shifts at specific times.

A to D shift is controlled by O-090, which is enabled by ERP2 when False, and ERP2 is False in Repeat function because Repeat FF is set. PS64 at O-090 will be False during EPC step 6. When both inputs to O-090 are False, the output is False and, applied through A-093 to I-094, is inverted True, designated RURR3 (A to D in Recall or Repeat). RURR3 True, applied through O-121 to I-122, is inverted False, designated SEAD4, and enables O-123. At the beginning of each B15 time TB154 goes False and O-123 output goes True to False. True to False transition of O-123 is inverted False to True by I-124 and applied through an emitter-follower as SAD9 to the counter circuits, which initiates an A to D shift each B15 time for all registers.

D to B shift is controlled by O-091, also enabled by ERP2 during Repeat function. PS64 will be False at O-091 during EPC step 6. TFG1 will be False during R1 through R4 time. TR13 is an inhibiting input on O-091 for R1 time when True. The result of these signals is to make O-091 output False for R2, R3, and R4 time only. False output of O-091 is applied through A-092 to I-096 and inverted True, designated RRRU3 (D to B in Recall or Repeat). RRRU3 True applied through O-128 to I-129 is inverted False, designated

SEDB4, and enables O-130. At the beginning of each B15 time TB154 goes False. Since SEDB4 is False only during R2, R3, and R4 time, TB154 can only transition O-130 output True to False for these times. True to False transition of O-130 is inverted False to True by I-131 and applied through an emitter-follower as SDB9 to the counter circuits, which initiates a D to B shift each B15 time for registers R2, R3, and R4.

The result of gates O-090 and O-091 on shifts of register data is to place R1 data in D Counter at the end of R1 time and simultaneously transfer R1 to B Counter (A to B) which preserves R1 data in the data sequence. TR13 at O-091 ensures no D to B shift at this time (R1B15) by causing SEDB4 to be True at O-130 for R1 time. However, SEDB4 True at I-125 does enable an A to B shift (SAB9 True). At the end of each R2 time, R2 data is shifted to D Counter and R1 data shifted to R2 time by the A to D, D to B shift. At the end of each R3 time, R3 data is placed in D Counter and R2 data placed in R3 time by the A to D, D to B shift. At the end of each R4 time, R4 data is placed in D Counter, and R3 data is placed in R4 time by the A to D, D to B shifts. R4 data is effectively discarded when the next RS data is shifted to D Counter by the A to D shift at the end of RS time. Note that while RS, R0, and R1 data is shifted A to D, this data is also shifted A to B, which preserves RS, R0, and R1 data in the data sequence. TFG1 at O-091 ensures no D to B shifts at RS and R0 time. Since there are no D to B shifts for these times, this data in D Counter is effectively discarded each A to D shift of new data. When all columns C1 through C14 have been shifted, HOME1 steps EPC to 7.

REPEAT - EPC7

No logic action occurs in EPC step 7 of Repeat, and the next HOME1 time steps EPC to 0.

REPEAT - EPC0

Logic action in EPC step 0 is exactly the same as in Add and Subtract functions, and uses the same logic. Repeat Function is completed.

7. RECALL

Recall function enables data placed in RS to be recalled to R1. Note that recalling RS data does not remove the data from RS, but only duplicates the RS data in R1.

RECALL - BEGIN

Pressing Recall Key (See Figure 2-36) closes Recall reed switch and, by means of CF code bar, also closes CF reed switch. Closing Recall reed switch enables an AC gate on Recall FF set input and 6 ms later EKBD3 at this gate sets Recall FF. Closing CF reed switch initiates KBD, unclamps EPC, and sets DPC exactly as in Add and Subtract functions previously discussed. (See Recall Flow Chart, Figure 2-37.)

RECALL - EPC1

As in Add and Subtract functions, and with exactly the same logic action, Display is inhibited, R1 is decimal aligned if not already aligned, and EPC steps from 1 to 6.

RECALL - EPC6

The logic action in EPC step 6 is to shift up RS data into R1 time, and at the same time shift up R1, R2, R3, and R4. Shift up of RS places RS data in R1 time, and shift up of R1 effectively clears R1 time for RS data insertion. The shift up of R4 effectively discards R4 data. Shift up is accomplished by A to D and D to B shifts at specific times.

A to D shift is controlled by O-089, which is enabled by ERC2 when False, and ERC2 is False in Recall function because Recall FF is set. PS64 at O-089 is False during EPC step 6. TRO3 is False except during R0 time, and acts to inhibit the A to D shift at R0 time. When all inputs to O-089 are False, the output is False and applied through A-093 to I-094 is inverted True, designated RURR3 (A to D in Recall or Repeat). RURR3 enables A to D shifts at all R times except R0, exactly as discussed in Repeat function EPC step 6.

D to B shift is controlled by O-088, also enabled by ERC2 during Recall function. PS64 at O-088 is False during EPC step 6. TFG1 will be False during R1 through R4 time. The result of these inputs is to make O-088 output False for R1 through R4 time during EPC step 6 in Recall function. False output of O-088 is applied through A-092 to I-096 and inverted True, designated RRRU3 (D to B in Recall or Repeat). RRRU3 enables D to B shifts at R1, R2, R3, and R4 times exactly as discussed in Repeat function EPC step 6.

The action of gates O-088 and O-089 on register data is place RS data in D Counter at the end of RS time, and simultaneously shift RS data to B Counter. The A to B shift of RS data preserves the RS data in the data sequence. The A to D shift of RS data stores the data for later insertion into the data sequence.

RO data is shifted A to B because A to D is

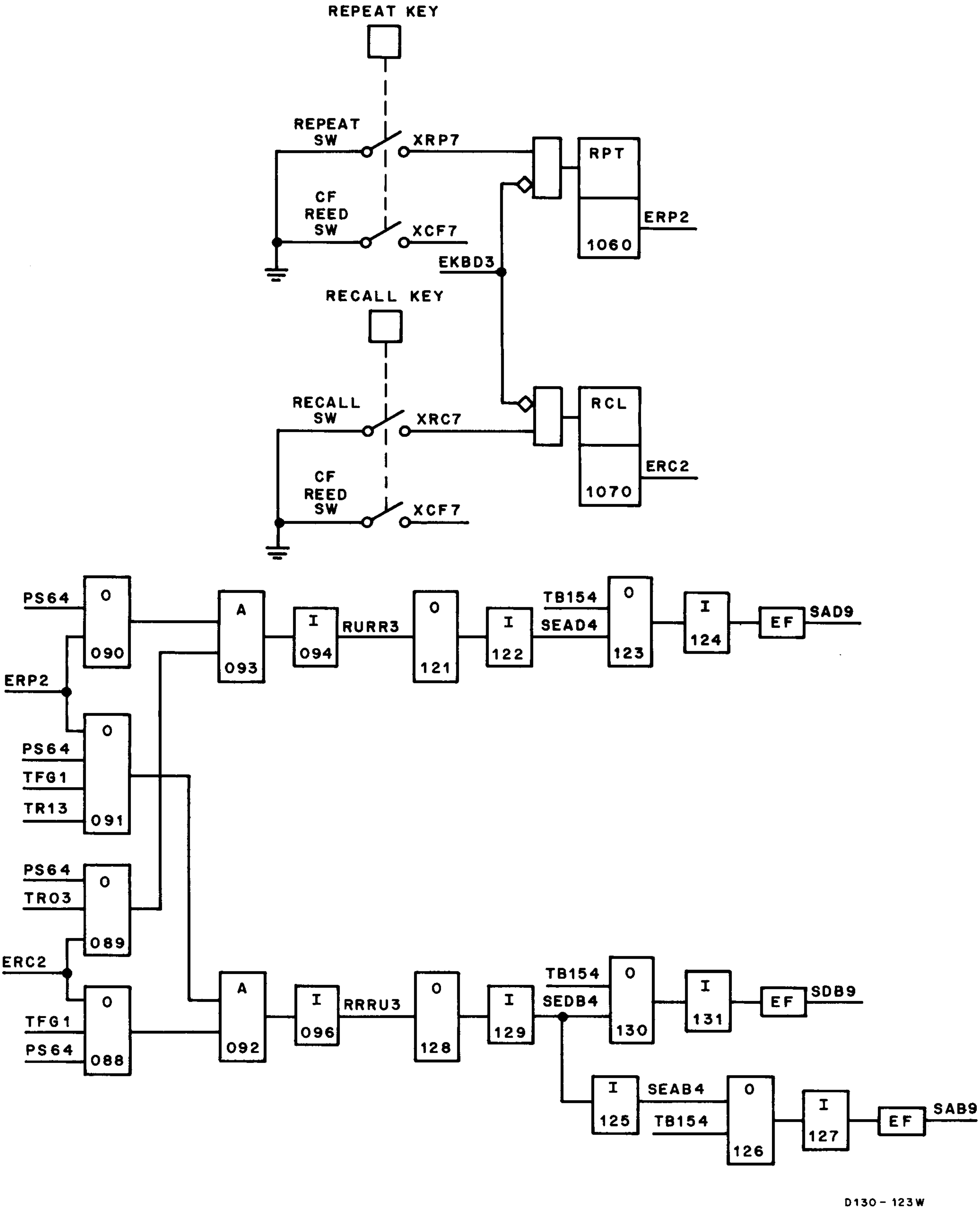


Figure 2-36. Repeat and Recall Logic

inhibited by TRO3 at O-089, which preserves the RO data in the data sequence. The inhibit of A to D for RO time preserves the RS data in D Counter since no new data is shifted in.

At the end of R1 time, R1 data is shifted A to D and D Counter data (RS data) is shifted D to B, which places the RS data in R1 time. At the end of R2 time, R2 data shifts A to D and D Counter data (R1 data) is shifted D to B, which places R1 data in R2 time. At the end of R3 time, R3 data shifts A to D and D Counter data (R2 data) is shifted D to B, which places R2 data in R3 time. At the end of R4 time, R4 data shifts A to D and D Counter data (R3 data) is shifted D to B, which places R3 data in R4 time.

At the end of the following RS time, RS data is shifted A to D and A to B simultaneously. When RS shifts A to B, D to B in inhibited, which discards the R4 data since RS data is now in D Counter and R4 data was not shifted out by a D to B shift.

The sequence of shifts starts with RS for each column time. When all columns, C1 through C14, have been shifted, HOME1 at O-024 steps EPC to 7.

RECALL - EPC7

No logic action occurs in EPC step 7 of Recall, and the next HOME1 time steps EPC to 0.

RECALL - EPC0

Logic action in EPC step 0 is exactly the same as in Add and Subtract functions, and uses the same logic gates. Recall function is completed.

8. STORE

Store function enables a number in R1 to be transferred to RS, which is undisplayed storage register.

Data stored in RS time is undisturbed by any functions except Clear All and Store. Clear All removes all data from the machine, which includes RS. Store replaces the data in RS with new data.

STORE- BEGIN

Pressing STORE Key (See Figure 2-38) closes Store reed switch and, by means of CF code bar action, also closes CF reed switch. Closing Store reed switch enables an AC gate at Store FF set input. 6 ms later EKBD3 at this gate sets Store FF. Closing CF reed switch initiates KBD, unclamps EPC, and sets DPC exactly as in Add and Subtract functions previously discussed. (See Store Flow Chart, Figure 2-39.)

STORE - EPC1

Display is inhibited, R1 is decimal aligned if not already aligned, and EPC steps from 1 to 6 exactly as discussed in Add and Subtract functions, EPC step 1.

STORE - EPC6

The logic action in EPC step 6 is to shift down R1 through R4, which places R1 data in R0 time in preparation for a succeeding shift down at EPC step 7 that will place the R0 data (previous R1 data) in RS time.

SHIFT DOWN

When Store FF sets, ESTO1 transitions False to True and sets Shift Down FF, which makes ESD2 False.

Shift down is controlled by O-084, which is enabled by ESD2 False. PS64 at O-084 is False during EPC step 6. TFG1 input to O-084 is False during R1 through R4 time. False output of O-084, applied through A-086 to I-087, is inverted True, designated RESD3 (enable shift down). RESD3 applied to I-118 is inverted False, designated SEAC4 (enable A to C shift), and enables O-119. TC153 input to O-119 is False from C1 through C14 time. TB154 input will be False at the beginning of B15 time for each register. The result of the inputs to O-119 is to make O-119 output False at the beginning of each B15 time for registers 1 through 4 at all C times except C15. False output of O-119, inverted True by I-120, is applied to the counter circuits as SAC9 to initiate A to C shifts for the times specified by TFG1 and TC153.

SEAC4 is also inverted True by I-115, designated SEBC4. SEBC4 when True inhibits O-116, which prevents B to C shifts when A to C shifts are specified. SEBC4 True is also applied through O-128 to I-129, inverted False, designated SEDB4 (enable D to B shift), and enables O-130. TB154 at O-130 goes False at B15 time, and the output of O-130 goes False each B15 time for R1 through R4 time at all C times. False output of O-130, inverted True by I-131, is applied through an emitter-follower as SDB9 to the counter circuits to initiate D to B shifts for the times specified.

SEDB4 is also inverted True by I-125, designated SEAB4. SEAB4 when True inhibits O-126, which prevents A to B shifts when D to B shifts are specified.

The result of the A to C and D to B shifts in

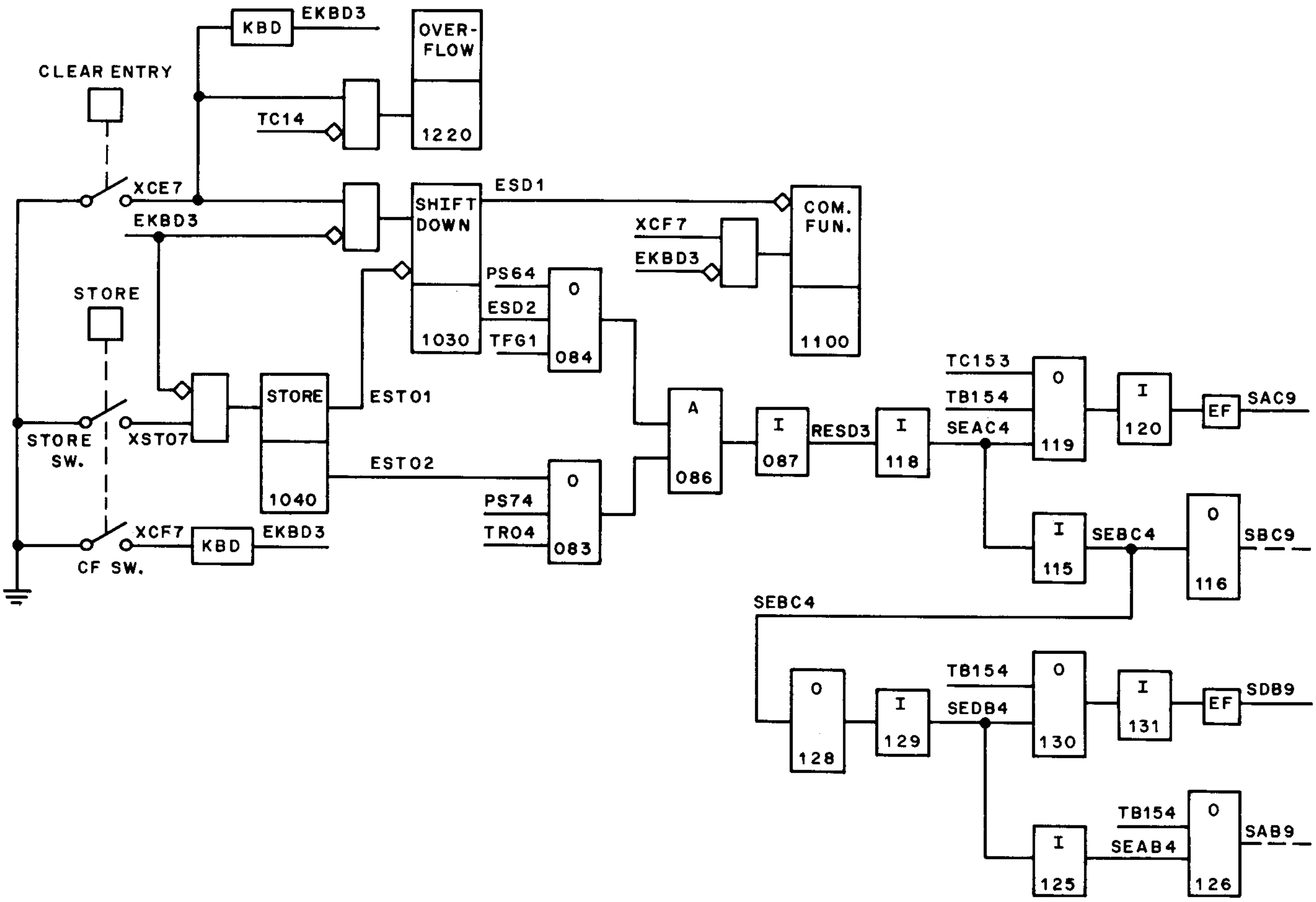


Figure 2-38. Clear Entry and Store Logic

EPC step 6 is to place R1 data in R0 time, R2 data in R1 time, R3 data in R2 time, and R4 data in R3 time. The D to B shifts in R4 time place zeros in R4 time, since there is no data to move into R4 time. The next HOME1 time at O-024 steps EPC to 7.

STORE - EPC7

The logic action in EPC step 7 is to shift down the data in R0, which is R1 data placed there in EPC step 6, to RS time.

The shift down of R0 data is controlled by O-083 enabled by ESTO2 being False because Store FF is set. PS74 at O-083 is False during EPC step 7. TRO4 at O-083 is False during R0 time. The result of the inputs to O-083 is to make O-083 output False during EPC step 7 during R0 time for all registers when Store FF is set. False output from O-083 applied through A-086 to I-087 is inverted True, designated RESD3. RESD3 True enables A to C and D to B shifts of data exactly as in EPC step 6, but for R0 time only. Thus, R0 data (previous R1 data) is shifted down to RS, which is the storage register. The next HOME1 time steps EPC to 0.

STORE - EPC0

Logic action in EPC step 0 is exactly the same as in Add and Subtract function, and uses the same logic gates. Store function is complete.

9. CLEAR ENTRY

Clear Entry function effectively erases R1 data, usually to permit a new number entry.

Clear Entry shifts R1 through R4 down one register. This places R1 information in R0 time. This is of no consequence because initiation of any arithmetical function will place new data in R0, replacing whatever data is already there.

Clear Entry function is similar to Store function in that a shift down of R1 through R4 data takes place in EPC step 6 and uses the same logic action and logic gates. However, in Clear Entry no further shift down in EPC step 7 is required or initiated. (See Clear Entry Flow Chart, Figure 2-39.)

CLEAR ENTRY - BEGIN

Pressing CLEAR ENTRY Key (See Figure 2-38) closes Clear Entry reed switch, which initiates KBD and also enables AC gates on Shift Down FF and Overflow FF.

The enable on Shift Down FF AC gate permits EKBD3, which was initiated by Clear Entry reed switch, to set Shift Down FF.

The purpose of the enable on Overflow FF reset input AC gate is to enable CLEAR ENTRY Key to remove keyboard lock-up at the same time R1 is being cleared if machine is in Over-Flow. If Overflow FF is set at the time Clear Entry function is initiated, TC14 going True at the end of C1 time provides a False to True transition that resets Overflow FF and removes keyboard lock-up as discussed in Keyboard function - Overflow logic.

Setting of Shift Down FF causes ESD1 to transition False to True. ESD1 is applied to set input of CF FF and sets CF. This method of CF set is different from usual set of CF which is by means of CF code bar and EKBD3. However, Clear Entry can also be used to correct a keyboard lock-up condition. If the keyboard was locked-up, CF code bar would also be locked-up and could not set CF directly, thus this method of CF set is necessary in a keyboard lock-up condition.

CLEAR ENTRY - EPC1

Display is inhibited, R1 is decimal aligned if not already aligned, and EPC steps from 1 to 6 exactly as discussed in Add and Subtract functions, EPC step 1.

CLEAR ENTRY - EPC6

The logic action in EPC step 6 is exactly the same as in Store function EPC step 6, and uses the same logic action and gates. The result of the logic action is to shift R1 through R4 down one register, which places R1 data, the register to be cleared, into R0 time. This data stays in R0 time, which is of no consequence since initiation of any arithmetic function replaces this data and it is effectively discarded. The next HOME1 time steps EPC to 7.

CLEAR ENTRY - EPC7

No logic action occurs in EPC step 7 of Clear Entry, and the next HOME1 steps EPC to 0.

CLEAR ENTRY - EPC0

Logic action in EPC step 0 is exactly the same as in Add and Subtract functions, and uses the same logic gates. Clear Entry function is completed.

10. CHANGE SIGN

The EC-130 performs all arithmetic operations in accordance with the rules of arithmetic in regard to signs. Since all entries are positive, a CHANGE SIGN Key is provided to make entries negative when desired. Also, answers with a negative sign may be made positive. CHANGE SIGN Key will reverse the sign of the number in register one.

C1 is reserved as the sign column for each register. No sign pulse in C1 time signifies that the number in the register is positive, and no sign is displayed. A Sign pulse in C1 time signifies that the number in the register is negative, and the sign pulse is decoded and displayed as a negative sign.

To change R1 sign from positive to negative, a sign pulse must be added to C1R1 time. To change R1 sign from negative to positive, the sign pulse must be removed from C1R1 time. This is done by adding another sign pulse to C1R1 time. This sets up an illegal code (2 setting) in B Counter at C1 time. The illegal code initiates logic which sets B Counter to 0. Since there is no sign pulse left in R1 time, this signifies a positive number and no sign is displayed.

CHANGE SIGN - BEGIN

Pressing CHANGE SIGN Key (See Figure 2-40) closes Change Sign reed switch and, by means of CF code bar action, closes CF reed switch. Closing Change Sign reed switch enables an AC gate on set input of Change Sign FF. 6 ms later EKBD3, which is initiated by CF reed switch, at this AC gate sets Change Sign FF. CF FF set initiates EPC unclamp and DPC set exactly as in Add and Subtract functions. The next HOME1 time steps EPC to 1.

CHANGE SIGN - EPC1

Display is inhibited, R1 is decimal aligned if not already aligned, and EPC steps from 1 to 6 exactly as discussed in Add and Subtract functions, EPC step 1.

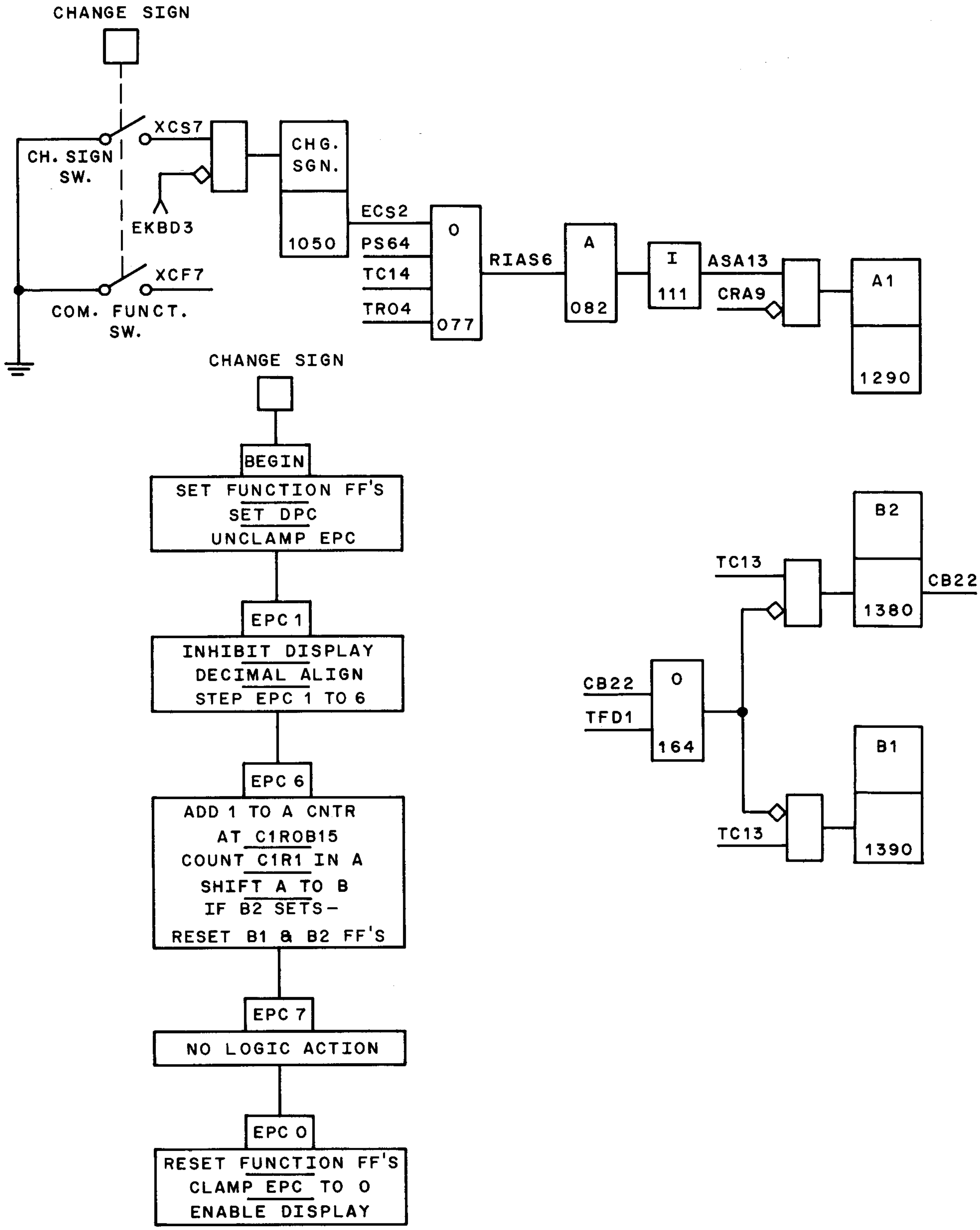


Figure 2-40. Change Sign Logic and Flow Chart

CHANGE SIGN - EPC6

Logic action in EPC step 6 is to add 1 to A Counter at C1R0B15 time and count C1R1 sign pulse into A on top of the 1 that was added. If R1 is negative, the count in A leaves A set to 2, and this 2 setting when shifted to B Counter initiates logic that cancels the setting. When B Counter is reset to 0 there is no sign pulse left in C1R1 time, and R1 sign has been changed from negative to positive. If R1 is positive, the count in A leaves A set to 1, and this 1 setting is shifted unchanged through the counters, which means there is now a sign pulse in C1R1 time, and R1 sign has been changed from positive to negative.

ADD 1 TO A

Add 1 to A is controlled by O-077, which is enabled by ECS2 being False when Change Sign FF is set. PS64 input will be False during EPC step 6. TC14 and TRO4 inputs will be False during C1R0 time. The result of the False inputs to O-077 is to make O-077 output False during C1R0 time and EPC step 6. False output of O-077, designated RIAS6 (increment A in sign), is applied through A-082 to I-111 and inverted True, designated ASA13 (enable set A1 FF). ASA13 is applied to enable an AC gate at set input of A1 Counter FF. When CRA9 (reset A Counter) is developed at B15 time (TB154 at O-140), A1 Counter is left in a set condition and A Counter counts up from a count of 1. Thus 1 is added to A at C1R0B15 time.

When C1R1 data from the delay line (CIA9) counts in A if C1R1 time contains a sign pulse then A sets to 2. If C1R1 time contains no sign pulse, then A stays set to 1 and this is now the sign of R1, which specifies R1 is negative.

RESET B COUNTER

Assume C1R1 did contain a sign pulse which set A to 2. Normal A to B shift places this 2 in B Counter, which means B1 and B2 are both set. When B2 sets, CB22 goes False and enables O-164. When TFD1, which specifies end of B7 time, goes False to True, the output of O-164 goes False to True. False to True transition of O-164 is applied to AC gates on B1 and B2 reset inputs that are enabled by TC13 being True during C1 time. The transition from O-164 resets both B1 and B2, which removes sign data from R1, and signifies R1 is now positive. Thus, R1 sign has changed from negative (sign pulse in C1R1) to positive (no sign pulse in C1R1). The next HOME1 time steps EPC to 7.

CHANGE SIGN - EPC7

No logic action occurs in EPC step 7 of Change Sign function, and the next HOME1 time steps EPC to 0.

CHANGE SIGN - EPC0

Logic action in EPC step 0 is exactly the same as in Add and Subtract functions, and uses the same logic gates. Change Sign function is complete.

11. CLEAR ALL

The EC-130 uses the principle of dynamic storage. That is, data to be preserved is constantly circulating through the counters onto the delay line and back through the counters (See Idle discussion).

An interruption of this data circulation means that the data will be erased. CLEAR ALL Key interrupts this data flow by inhibiting the action of the Write Amplifier, which effectively clears (erases) all data from the machine since no data is written on the line while the Write amplifier is inhibited.

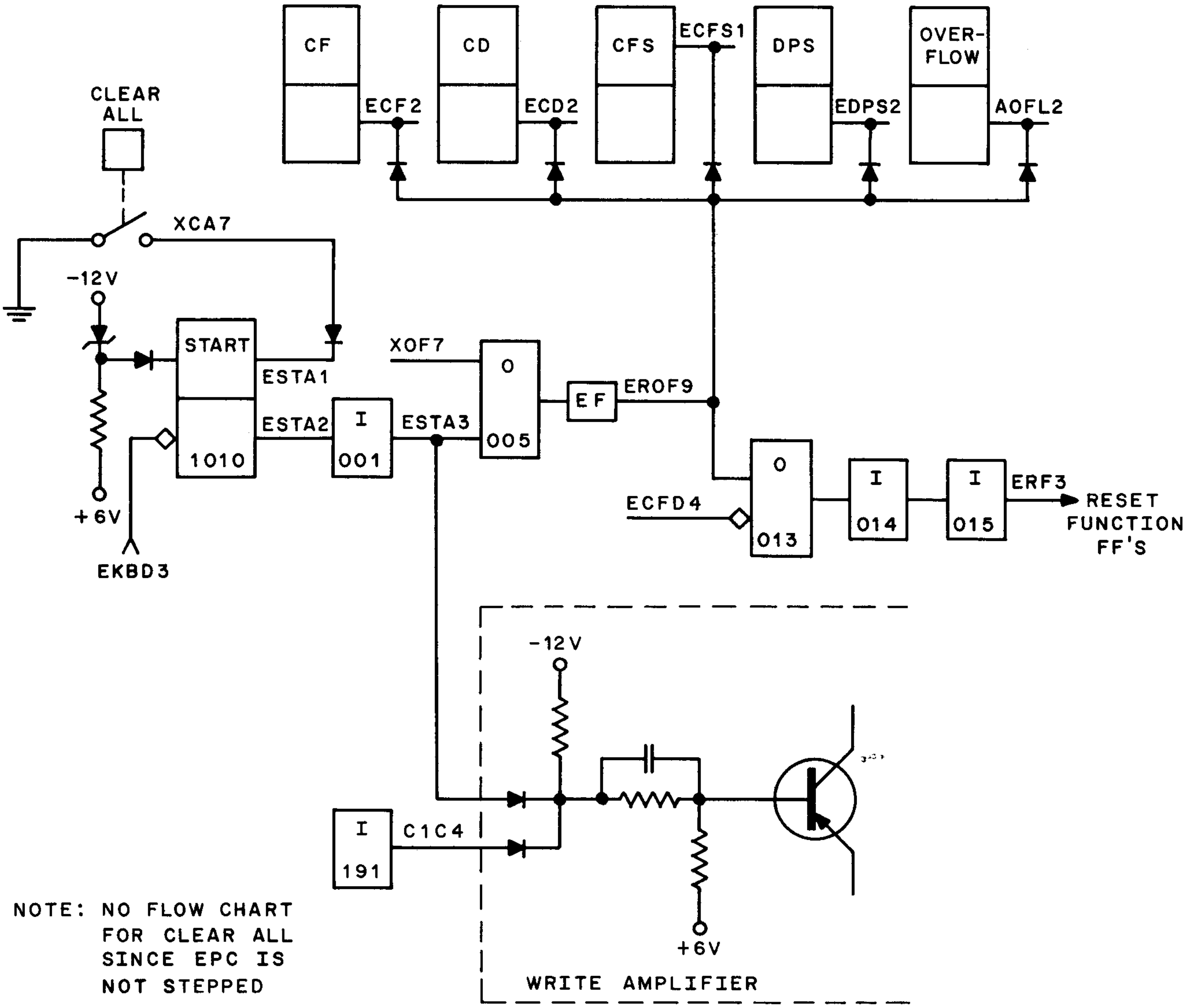
Pressing CLEAR ALL Key (See Figure 2-41) closes Clear All reed switch, which through an isolation diode places effective ground at the set output of Start FF, and Start FF sets. Set of Start FF makes ESTA2 False, which is inverted True by I-001, designated ESTA3. ESTA3 True is applied through O-005 and an emitter-follower as EROF9 to clamping diodes on reset output of CF, CD, DPS, and Overflow FF's and clamps those FF's reset. EROF9 applied through an isolating diode also clamps CFS FF to set.

At the same time, EROF9 is applied through O-013 to I-014 and inverted False, then inverted True by I-015, designated ERF3. ERF3 True applied to clamping diodes on the reset outputs of the function FF's clamps all function FF's to reset.

One of the results, then, of ESTA3 going True is to set CFS FF and reset all other function FF's. This prepares the machine for the entering of new data.

ESTA3 True is also applied as one input to an OR gate at the Write Amplifier. The action of this OR gate is covered in Write Amplifier discussion. However, when ESTA3 is True at this gate, the output is True, and the Write Amplifier input transistor is biased off. As long as this transistor cannot change state, no data is written on the line. As long as ESTA3 is True, the data pulse input, designated CIC4, can have no effect on the Write Amplifier thus writing data onto the delay line is inhibited by ESTA3.

To clear the inhibit at the Write Amplifier, ESTA3 must go False. This is accomplished by reset of Start FF by EKBD3 when the initiation of any function closes either CF or CD reed switches, which initiate KBD. 6 ms (approximately) after KBD is initiated, EKBD3 goes True and resets Start FF. When Start FF resets, ESTA2 goes True and ESTA3 goes False. ESTA3 False removes the inhibit on the OR gate at the Write Amplifier and also, through O-005, removes the diode clamping action at CD, CF, and the other FF's clamped to reset by EROF9.



NOTE: NO FLOW CHART FOR CLEAR ALL SINCE EPC IS NOT STEPPED

Figure 2-41. Clear All Logic

I. DISPLAY DEFLECTION

The deflection circuits develop the voltages that are applied to the deflection plates to move the spot caused by the electron beam and form the characters on the screen in their proper position. The voltages applied to the deflection plates are developed by combining separate voltages from the Segment Generator, Horizontal and Vertical Dot Generators, and Horizontal and Vertical Staircase Generators. The horizontal deflection voltage is slightly modified by the slant amplifier. To attain necessary voltage levels at the deflection plates, the horizontal and vertical deflection voltages are amplified by horizontal and vertical amplifiers after development.

The deflection voltages are continuously generated whether the machine is in display or not. In other words, the deflection circuits are developing display positioning voltages at all times the machine is on, but the blanking circuits permit only the desired data to be displayed.

A composite block diagram of the deflection circuits is illustrated in Figure 2-42, and each block will be covered separately.

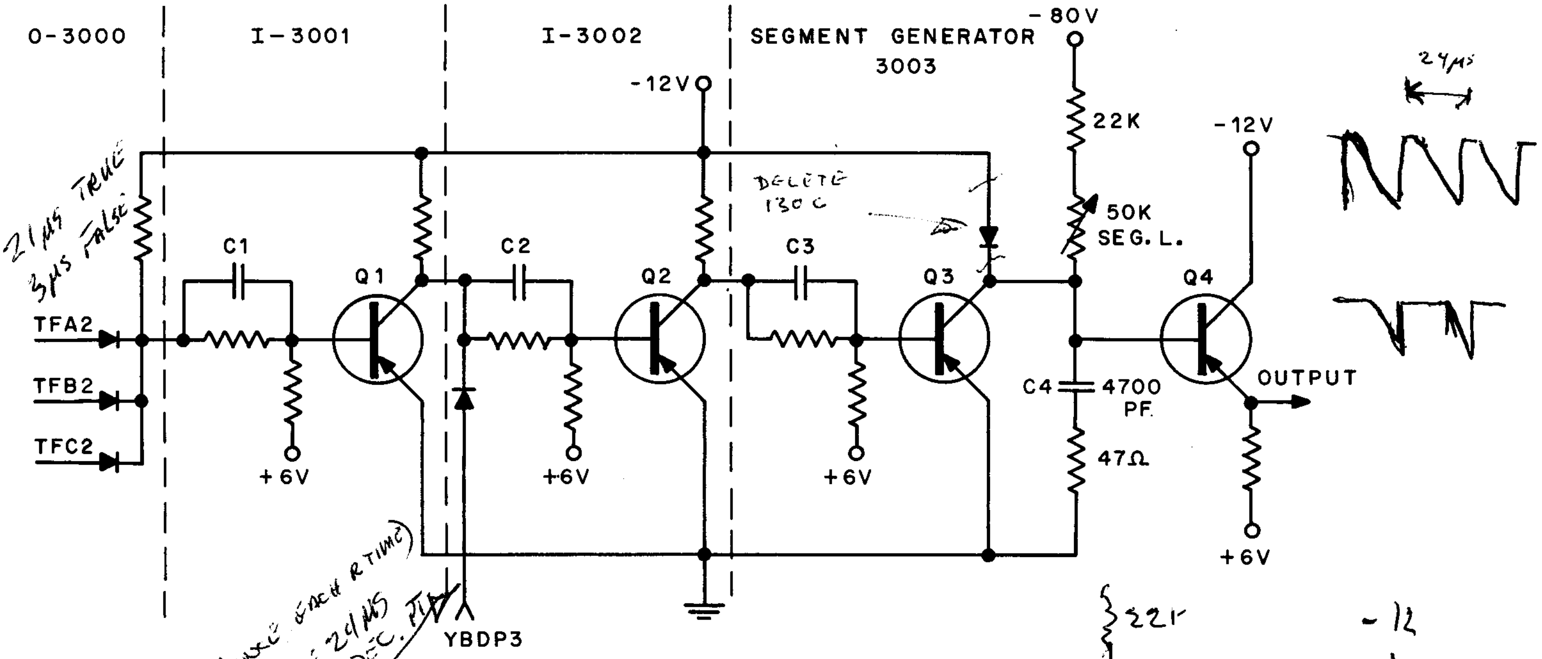
1. SEGMENT GENERATOR

The segment generator produces the basic deflection voltage that will draw a segment of a character on the CRT screen. There are twelve (12) segments produced, not all of which are used.

The development of the deflection voltages starts with the Segment Generator (Figure 2-43). A segment is a portion of a character and there are 12 segments produced each 288 µsec. Certain numbered segments form the basic figure 8. While all segments are produced, the blanking circuits determine which will be displayed, thus which character will be formed on the CRT. The purpose of the segment generator circuit is to produce a linear sawtooth sweep that will ultimately be applied to the CRT deflection plates.

The diodes at the base input of Q1 form an OR gate, which means that if TFA2 or TFB2 or TFC2 are True, the output is True, and Q1 is biased off. If Q1 is off, the collector is -12 volts, which applied to Q2 turns Q2 on. If Q2 is on, then the collector of Q2 is essentially 0, which applied to Q3 turns Q3 off. When Q3 is off, C4 starts to charge toward -80 volts through the 50K variable resistor and 22K in series. The RC time of charge can be varied by the 50K potentiometer between approximately 338 µsec and 103 µsec.

TFA2, TFB2, and TFC2 at the diode gate will all be False together for 3 µsec of each 24 µsec (see Bit Counter discussion). When TFA2 and TFB2 and TFC2 are False the diode gate acts as a -AND, and the base of Q1 goes negative, Q1 turns on and Q1 collector goes essentially to ground. Q1 collector going to ground changes the voltage at the base of Q2 to positive, and Q2 turns off. Q2 off means Q2 collector goes to -12



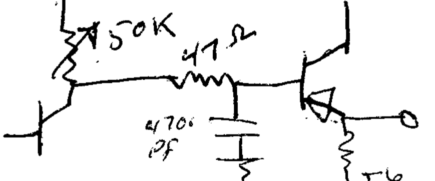
21µs TRUE 3µs FALSE

DELETE 130 C

24µs

(LEAVE EACH R TIME) TRUE 24µS FOR DEC. PT.

Figure 2-43. Segment Generator Schematic



volts, which turns Q3 heavily on, and Q3 collector goes effectively to ground. Whatever charge C3 has accumulated during 21 µsec will discharge very quickly through Q3 and the 47 ohm current limiting resistor.

C4, then, can charge for 21 µsec and then discharge for 3 µsec. Since the charge path is long, the time that C4 can charge (21 µsec) is less than 10% of RC time, and the voltage rise of C4 is essentially linear. However, varying the 50K potentiometer will change the voltage level C4 charges to by varying RC charge time, thus the amplitude of the developed sawtooth waveform can be varied. The sawtooth rise of C4 voltage is applied to emitter follower Q4, and the emitter of Q4 will follow this waveform, which is the output of the Segment Generator.

Decimal Point signal, YBDP3, is applied to a diode at the base voltage divider of Q2, where the collector of Q1 is also connected. If YBDP3 is True Q2 is turned off. YBDPS3 is True for 24 µsec when decimal point is desired, thus Q2 is turned off for 24 µsec instead of 3 µsec as in normal segment generation. Q2 off means Q3 on, and when Q3 is on C4 is not charging. One segment is thus effectively cancelled by decimal point, and this is arranged to be always segment 13 by YBDP3 logic. If the CRT spot does not move because there is no sweep at a given segment 13 time, a spot is formed at that point on the scope face. Decimal point (YBDP3 True) occurs only once for each register display, therefore, only one decimal point will be displayed in a register.

2. SEGMENT SWITCHING CIRCUITS

Certain of the 12 segments are used to develop a horizontal sweep, and the other segments to develop a vertical sweep. The circuits which designate the application of the Segment Generator output sawtooth to the Horizontal or Vertical sweep channels are called Segment Switching Circuits, sometimes Diode Switches. (See Figure 2-44.)

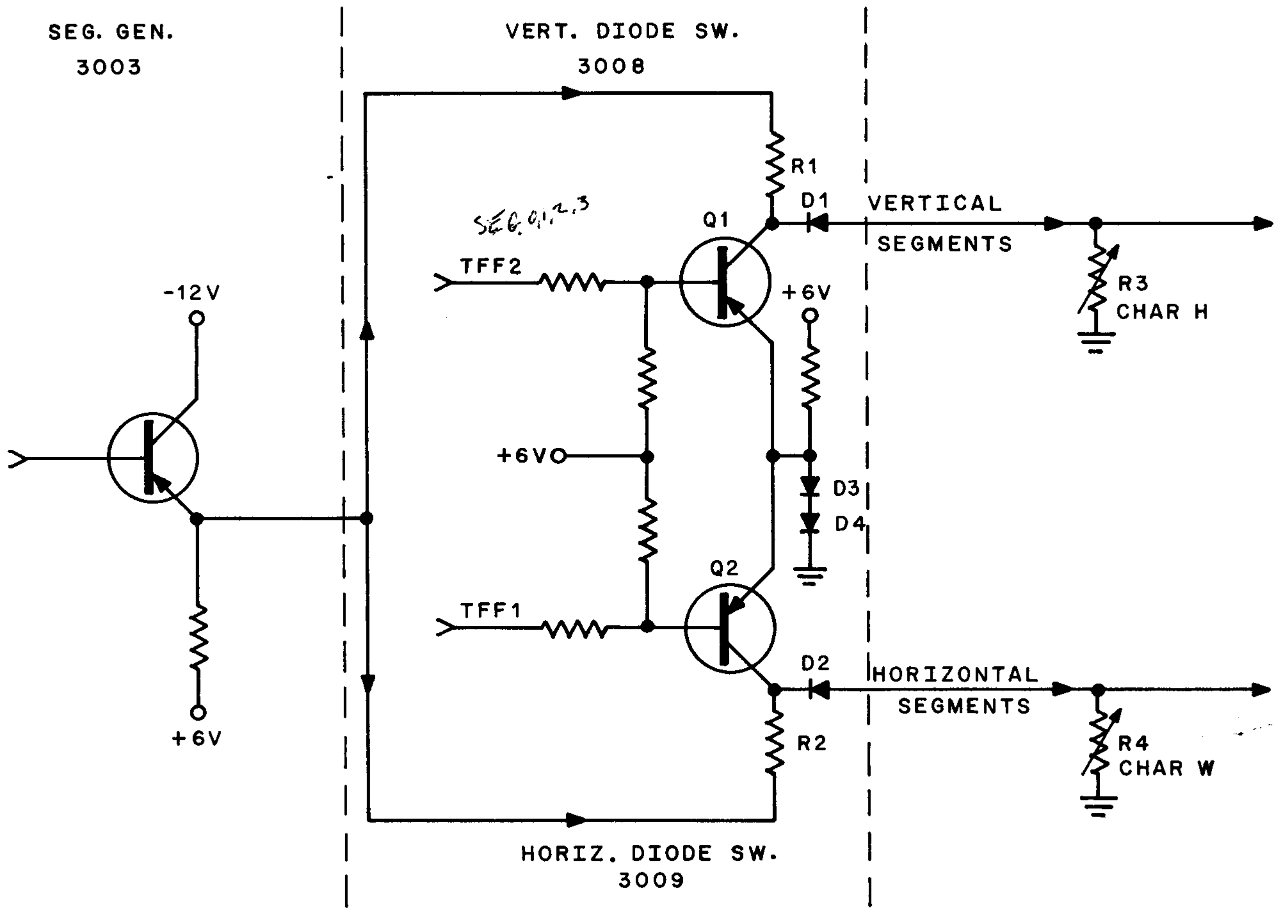


Figure 2-44. Segment Switching Schematic

The negative going segment sweep waveforms are applied to the cathodes of D1 and D2 through R1 and R2, which are also the collector resistors of Q1 and Q2. The bias network at the emitters of Q1 and Q2 establishes approximately 1 volt fixed bias due to the forward bias drop across D3 and D4. Assume TFF2 to be False (-12 volts), Q1 turns heavily on and the +1 volt on Q1 emitter appears at the collector and biases D1 off, thus no segment sweeps are coupled to R3 and no Vertical sweeps. If TFF1 is False, which will be when TFF2 is True, then Q1 is off and Q2 is on, thus D2 is biased off and no horizontal sweeps are permitted. Therefore, TFF2 and TFF1 are used to switch the segment waveform from the Vertical to the Horizontal channel, and vice-versa.

TFF2 will be True for segments 0, 1, 2, and 3 and False for all others, therefore those segments will be applied to the vertical channel. Since TFF1 is False when TFF2 is True, no sweeps are permitted into the horizontal channel for segments 0, 1, 2, and 3. Examination of the character formation diagram (Figure 2-49) shows that vertical segment displacement of the sweep is necessary only during segments 0, 1, 2, and 3.

TFF1 will be True for all sweeps other than 0, 1, 2, and 3, thus Q2 is cut-off permitting the segment sweeps to be coupled through D2. When TFF1 is True, TFF2 is False and Q1 is conducting, which biases D1 off and blocks the segment sweeps from the vertical channel.

Variation of Character Height potentiometer establishes the amplitude of the vertical segments at this point and therefore the final vertical segment sweep for these segments. Character Width potentiometer establishes the final horizontal segment sweep for the horizontal segments.

3. DOT GENERATORS

The horizontal and vertical dot generators develop voltage levels that position the CRT beam for the beginning of a segment trace. (See Figure 2-49.)

As illustrated, a vertical segment may begin at vertical level A or B and at horizontal level D or E. Thus, there are four possible starting points for drawing a vertical segment. For example; Segment 0 would start at vertical level A, horizontal level E: Segment 3 would start at vertical level B, horizontal level D: etc.

A horizontal segment may begin at vertical levels A, B, or C and horizontal levels D, E, or F. Thus there are six possible starting points for drawing a horizontal segment. For example; segment 6 would start at vertical level A, horizontal level D: segment 15 at vertical level C, horizontal level D: etc.

a. The vertical dot generator, Figure 2-45, is a voltage divider network between -8 volts and ground. The zener in series with the resistor to -12 volts provides regulated -8 volts to the voltage divider.

4 STARTING POINTS (VERT) ARE A & B.

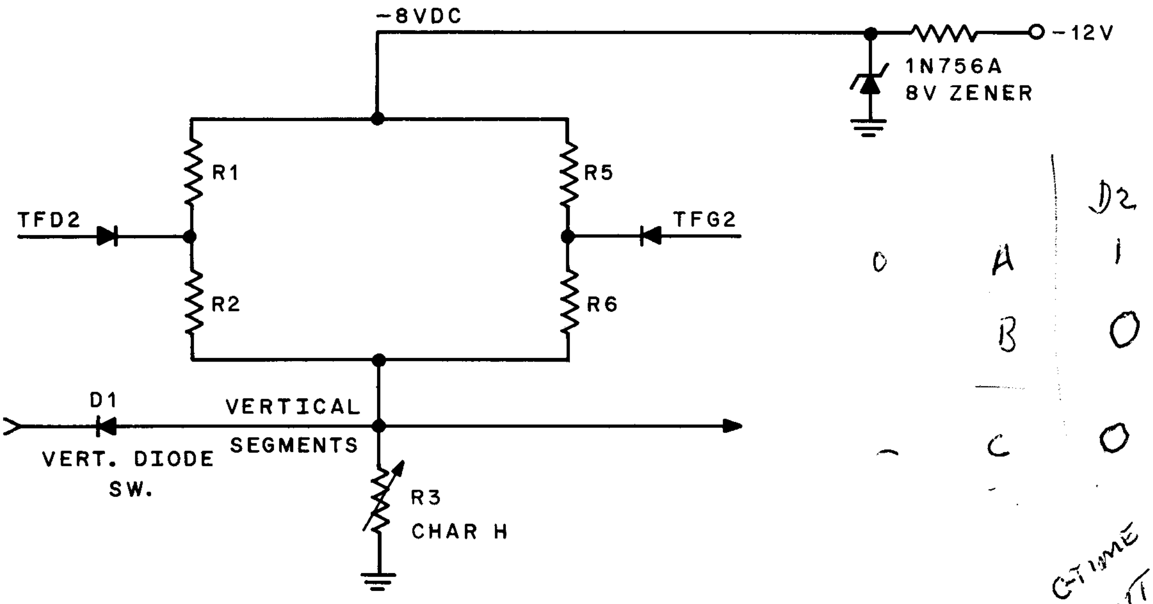


Figure 2-45. Vertical Dot Generator Schematic

		D2	G2
0	A	1	1
	B	0	1
–	C	0	0

WITHIN G-TIME V.D.G. SWITCHES BETWEEN A&B

R1, R2, R5 and R6 are all equal. There are three vertical levels that must be specified for the character construction (See Dot Generator Levels diagram.) The voltage divider establishes a DC level at the top of R3 from which the segment sweep voltage varies. Three conditions of the voltage divider are determined by TFD2 and TFG2. Level A, the least negative, is when TFD2 and TFG2 are both True (0 volts). The junctions of R1-R2 and R5-R6 are at 0 volts (ground), thus no negative voltage at the top of R3 and the segment sweep varies from ground to a more negative level. Level C, the most negative, is when TFD2 and TFG2 are both False (-12 volts). The isolating diodes are both back-biased and effectively out of the circuit. The DC level at the top of R3 will be established only by the ratio of the resistances in the voltage divider, and will be at the most negative level, from which the segment sweeps will vary. Level B is a point between the most positive and most negative level. If TFG2 is True and TFD2 is False, then the junction of R5 and R6 is at 0 (ground) and the voltage at the top of R3 is determined by the ratio of R1 and R2 in series with R6 and R3 in parallel to ground. This will be less negative than condition C, and more negative than condition A, and is designed to be approximately between the two. During the time level B is desired, either TFG2 or TFD2 will be True (-0 volts) which will give condition B.

b. The Horizontal Dot Generator, Figure 2-46, functions similarly to the Vertical Dot Generator but the voltage divider is not symmetrical, thus the voltage division steps will not be equal.

R1 and R2 are equal and R5 and R6 are equal. There are three horizontal levels that must be specified for the character construction (See Dot Generator Levels diagram). The voltage divider establishes a DC level at the top of R4 from which the segment sweep voltage varies. Three conditions of the voltage divider are determined by TFG2 and TFE1. Level D, the least negative is when TFE1 is True (0 volts). The junctions of R1-R2 and R5-R6 are at 0 volts (ground), thus no negative voltage at the top of R4, and the segment sweep varies from ground to a more negative level. Level F; the most negative is when TFG2 and TFE1 are both False (-12 volts). The isolating diodes are back-biased and effectively out of the circuit. The DC level at the top of R4 is established only by the voltage divider resistances, and will be at the most negative level, from which the segment sweeps will vary, (which will place Decimal Point (Segment 13) slightly to the left of a normal character 8).

Level E is a point between the most positive and the most negative level and develops when TFG2 is True and TFE1 is False. TFE1 isolaing diodes are back-biased and effectively out of the circuit but TFG2 isolating diode is forward biased, and the junction of R1 and R2 is at 0 volts (ground). The voltage at the top of R4 is determined by R5 and R6 in series with R4 and R2 in parallel to ground. This will be less negative than condition F, and more negative than condition D.

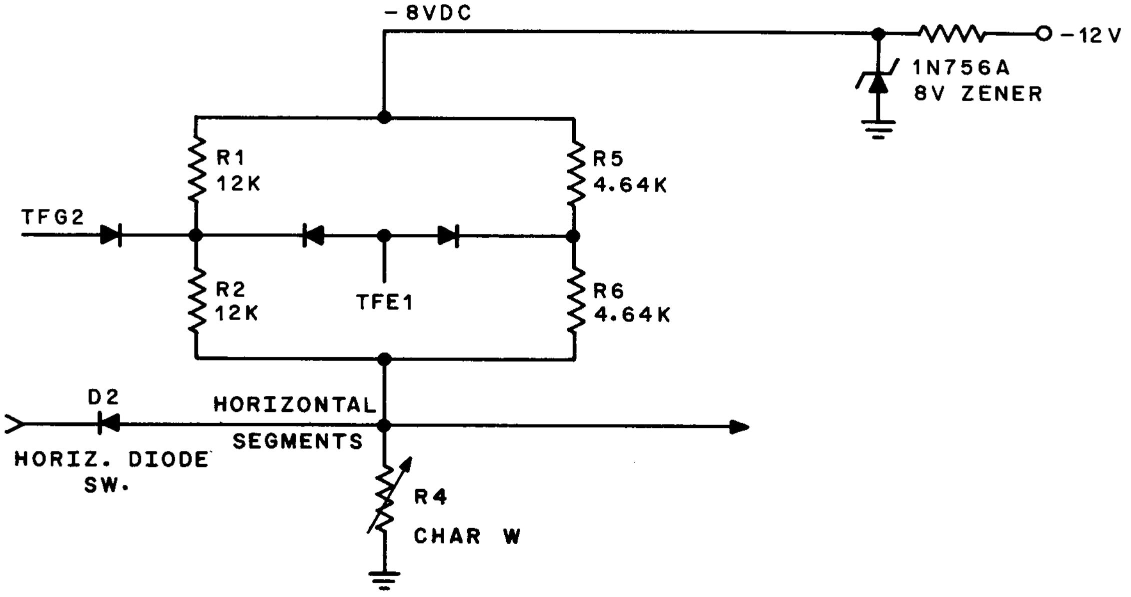


Figure 2-46. Horizontal Dot Generator Schematic

4. SLANT AMPLIFIER

The slant amplifier provides an offset voltage, derived from the vertical deflection and applied to the horizontal deflection, to slant each vertical segment for a more pleasing display. Each vertical segment is slightly offset at the bottom compared to the top.

The slant amplifier (Figure 2-47) is a simple one transistor circuit with the base connected in the vertical sweep channel. As the vertical segment sweep goes in a negative direction, the base of the transistor goes negative, and the transistor conducts more heavily. As the transistor draws more current, the junction of the 2.2K and 680 ohm resistor goes more negative. This negative change is applied to the Horizontal Staircase Emitter-follower. Effectively, this adds a negative voltage to the horizontal deflection plates and the bottom of each vertical segment will be displaced, or slanted, to the left as compared to the start of the segment.

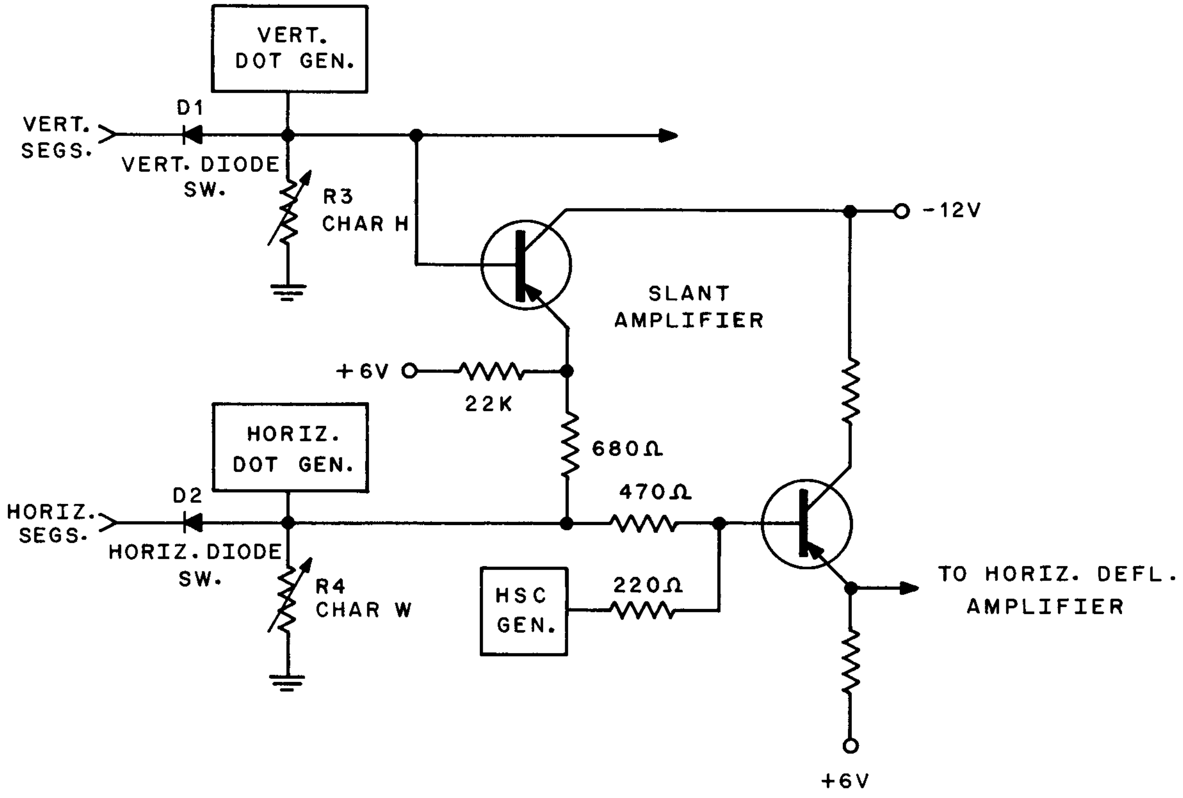


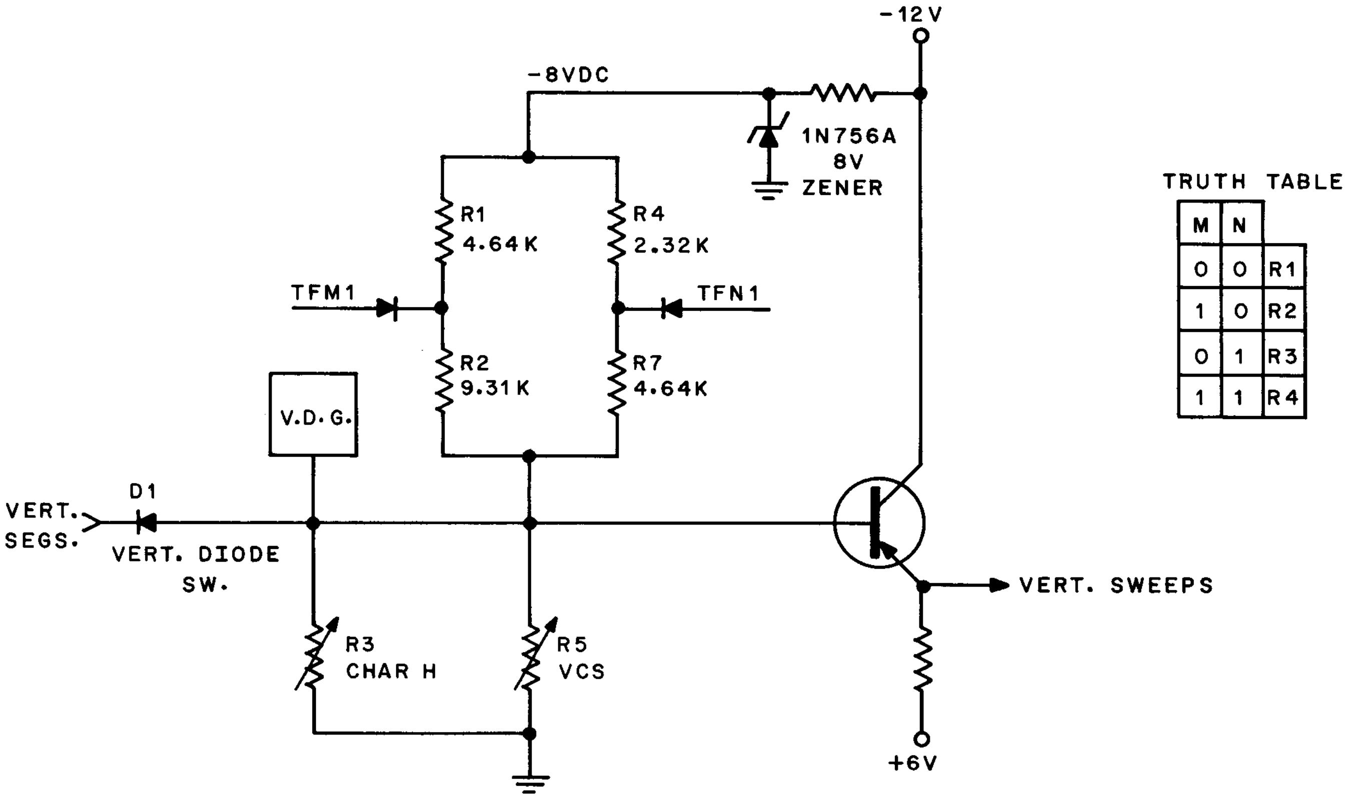
Figure 2-47. Slant Amplifier Schematic

5. VERTICAL STAIRCASE GENERATOR

The Vertical Staircase Generator develops four (4) voltage levels that position the characters in the proper register. (See Figure 2-48.)

The Vertical Staircase Generator is composed of a voltage divider very similar to the Dot Generator. However, since there are four registers to be positioned, there must be four voltage levels developed (See Deflection Voltage Relationships diagram).

M and N display timing FF's change state each word time in a specific sequence. (See Display Timing discussion.) A given state of M and N FF's delineates a specific register (See Truth Table), and they will remain in that state for all display column times for that register (C1 through C14). In other words, R1 is displayed for each column, then R2, then R3, and finally R4. Since M and N FF settings delineate specific registers, then M and N settings are used to control vertical positioning voltages that will display those registers in the proper place on the CRT.



M	N	
0	0	R1
1	0	R2
0	1	R3
1	1	R4

Figure 2-48. Vertical Staircase Generator Schematic

Assume M and N are both reset. This designates R1 and, since R1 is the lowest register, the vertical staircase must be the most negative at this time. When M and N are in reset state, M set output (TFM1) and N set output (TFN1) will be False (-12 volts). M and N isolating diodes in the voltage divider are back-biased and effectively out of the circuit. The voltage at the top of R5 will be determined only by the voltage divider ratio of resistances, and will be the most negative. The segment sweeps, as conditioned by the Vertical Dot Generator and Character Height (R3), will vary from this point.

Now assume M set and N reset. This designates R2 time and, since R2 is the next register up from R1, the vertical staircase start must be somewhat less negative during this time. TFM1 is True and TFN1 is False. TFN1 isolating diode is back-biased out of the circuit, thus that leg of the voltage divider is not affected. However, TFM1 being True forward biases TFM1 isolating diode and the junction of R1 and R2 goes to 0 (ground).

The -8 volts is now divided between R4 and R7 in series with R5 and R2 in parallel to ground, and the voltage at the top of R5 is less negative than during R1 time.

With M reset and N set, R3 time is designated. TFM1 diode is now back-biased and out of the circuit, while TFN1 diode is forward biased and the junction of R4 and R7 is at 0 volts (ground). The voltage division is now between R1 and R2 in series with R7 and R5 in parallel to ground and the voltage at the top of R5 is less negative than during R1 and R2 time.

With M and N both in set state, TFM1 and TFN1 diodes are both forward biased and 0 volts is at the junction of R1-R2 and R4-R7. Thus, no negative voltage from the voltage divider, and the top of R5 is 0 volts (ground) and the segment sweeps, conditioned by R3 setting and the Vertical Dot Generator, vary from that point, which is the least negative condition.

The composite vertical segment sweeps have now been developed and are applied through an emitter-follower to the Vertical Deflection Amplifier.

6. HORIZONTAL STAIRCASE GENERATOR

The horizontal staircase generator produces the voltage levels that ultimately position the 13 digits and the sign on the display. To do this requires 14 separate, distinct levels. Since each character (digit) time is 288 µsec, it follows that each voltage level is 288 µsec long. If there are 14 steps of 288 µsec each, then the overall staircase waveform is 14 x 288 µsec or about 4.03 milliseconds long. The waveform, with respect to time, will look as illustrated in Deflection Voltage Relationships diagram.(See Figure 2-49.)

The basic action of the Horizontal Staircase Generator is to charge up a capacitor by steps, with special precaution being taken that no discharge of the capacitor (sagging) occur between steps. (See Figure 2-50.)

The input to the Staircase Generator is an OR gate, which acts as a -AND. YCPR4 will be False for 48 µsec in each 288 µsec, TFD2 will be False during the last 24 µsec of YCPR4, and SAD9 will be False except for the last 3 µsec of YCPR4. Thus the input to the -AND gate will look as illustrated in the waveforms.

When any input to the OR gate is True, the output is True and the gate side of C1 is at 0 volts. The other side of C1 is at the base to emitter voltage of Q1. Since Q1 is biased heavily on, the base to emitter voltage is approximately 0 volts.

When all inputs to the OR gate are False, the gate acts as a -AND, and the output is False. C1 then sees a transition to -12 volts on the input

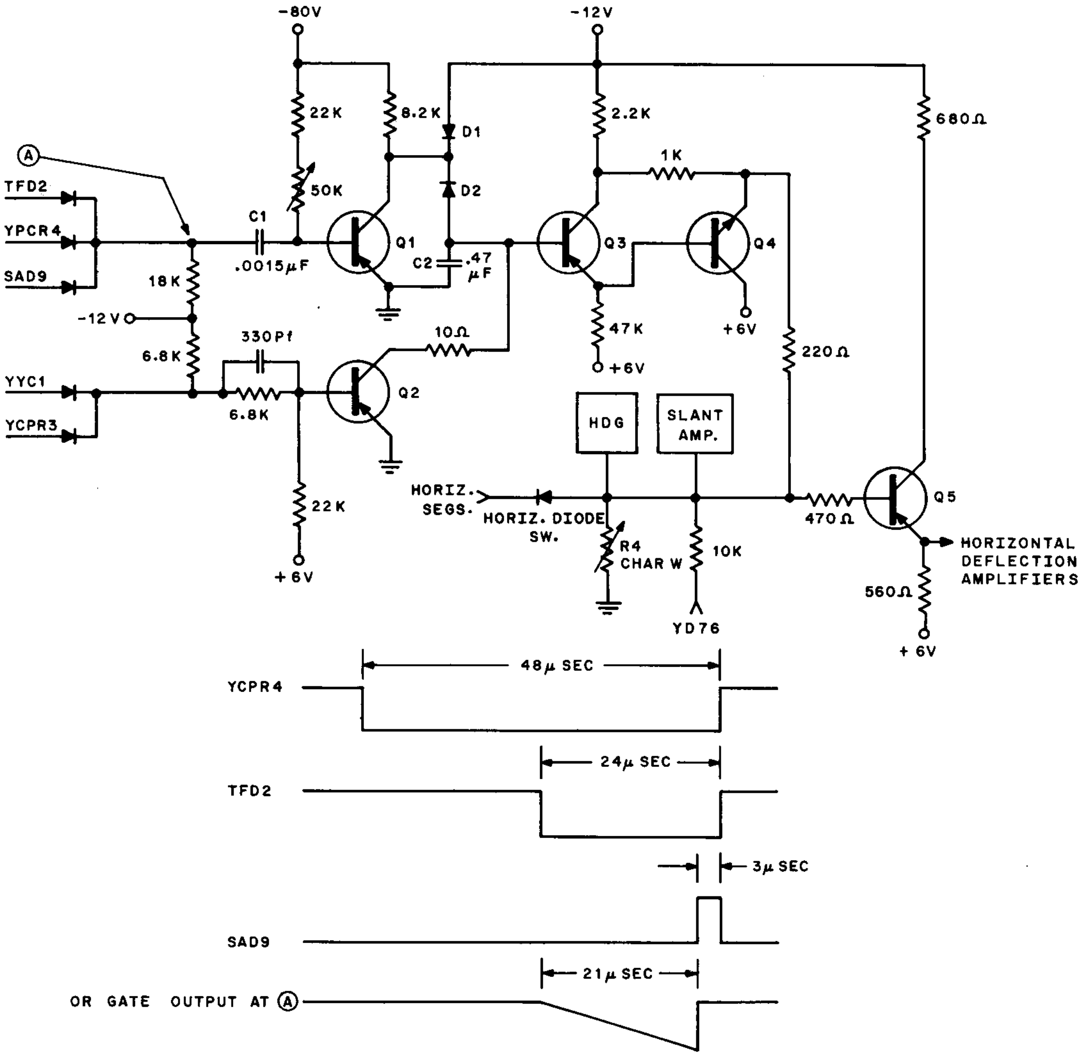


Figure 2-50. Horizontal Staircase Generator Schematic

side with 0 volts still on Q1 side, and charges toward this -12 volts for 21 μsec, which is the length of time the OR gate output is False. C1 charges to approximately 6.5 volts in this length of time. Now, one input (SAD9) of the OR gate goes True, the output goes True, and C1 must discharge. This positive transition of about 6.5 volts is coupled to the base of Q1 and turns Q1 off. With Q1 off, Q1 side of C1 no longer is at 0 volts, and must charge toward -80 volts through the 50K variable potentiometer, 22K, and 18K.

Q1 cannot turn on again until the base again becomes negative, and the base cannot become negative until Q1 side of C1 has time to change appreciably negative through the long RC time charge path. This means that the length of time Q1 will be off is a function of this RC time, and the time can be varied by the 50K potentiometer.

Therefore, the function of the gate is merely to allow time for C1 to charge to an adequate value at a specific time, then, when any input goes True, Q1 turns off. The length of time Q1 is off is then a function of RC time of charge of C1, which can be varied by the 50K potentiometer.

When Q1 is on, Q1 collector is essentially at 0 volts and D1 and D2 are back-biased. Thus C2 has ground on one side, and is open circuited on the other (through D2), therefore, no charge on C2 at this time. Now assume Q1 is turned off by action of the gate. Q1 collector is returned to -80 volts, and will go negative. When Q1 collector goes negative, D2 is immediately forward biased and C1, then, is connected to -80 volts through the 8.2K collector resistor. C2 can charge as long as Q1 is off, and this, in turn, is determined by the setting of the 50K potentiometer.

The amount that C2 can charge is a function of how long it is allowed to charge and the RC time of the charge path. Since the charge path is fixed, being the 8.2K collector resistor, the only variable is the time Q1 is off. Assume that for a given setting of the 50K potentiometer C2 charges up to .1 volts.

Now Q1 turns on. When Q1 is on, the collector is at 0 volts (essentially), and this back-biases D2, which open circuits the connection between C2 and -80 volts. Thus, C1 cannot lose any charge. Q3 and Q4 comprise a special emitter-follower arrangement that enables C2 voltage level changes to appear as horizontal staircase output without affecting the charge on C2. See Lesson 22 of FRIDEN Electronic Course for a fuller explanation.

Q1 will be on for the rest of the 288 μsec because YCPR4 goes False only once in each 288 μsec. When YCPR4 goes False again, Q1 turns off and C2 can then charge to a higher value, which will be approximately .1 volts each time, or .1 volts per step of voltage.

The purpose of D1 connected between the collector of Q1 and -12 volts is protection for Q1 in case Q1 was off long enough for more than -12 volts to appear at the collector. Normally D1 is always back-biased because the maximum potential C2 can charge to in 14 steps is 14 x .1, which is about 1.4 volts. However, should a malfunction occur which might tend to raise the collector of Q1 to -80 volts, then D1 conducts when Q1 collector reaches -12 volts, and this clamps Q1 collector to -12 volts, protecting Q1.

C2 is allowed to step for fourteen (14) column times, then discharge very quickly and the stepping process repeated. The discharge of C1 is controlled by Q2, the Horizontal Staircase Reset. The input to Q2 is a diode OR gate. If either input is True, the output is True, which places the junction of the diodes with the base voltage divider at 0 volts. Q2 is biased off because the base is positive. With Q2 off, C2 cannot discharge through the 10 ohm current limiting resistor and Q2.

When Display Control (FF) set output (YYC1) is False and YCPR3 is False, the output of the diode gate is False and -12 volts is connected into the voltage divider. The ratio of the resistances is such that Q1 base goes negative, which biases Q2 heavily on. When Q2 is on, Q2 collector is essentially at ground. At this time C2 is connected essentially to ground through 10 ohms and discharges very quickly. The 10 ohm resistor is to limit current flow through Q2, which is in C2 discharge path to ground.

When either YYC1 or YCPR3 input go True, the output of the diode gate is True (0 volts) and Q2 is turned off by the voltage divider action, which places Q2 base positive.

The Horizontal Staircase output is from the emitter of Q4, and is applied to emitter-follower Q5. The horizontal segment sweeps as conditioned by the Horizontal Dot Generator and the Slant Amplifier also are applied at the base of this emitter-follower. The output of the emitter-follower is applied to the Horizontal Deflection Amplifier.

7. DEFLECTION AMPLIFIERS

When the respective voltage levels of the Segment generator, the Dot generators, the Staircase generators, and the Slant Amplifier have been combined to give the character formation and placement, the combination is amplified to the necessary voltage levels for the CRT deflection plates by the deflection amplifiers.

While the deflection signals are very complex waveforms, at any moment they are only the algebraic addition of several simple waveforms. For instance, the horizontal deflection signal must move the beam to 14 distinct locations for each register (Horizontal Staircase Generator); within that location start the beam at a specific point (Horizontal Dot Generator): and move the beam horizontally from that point (Horizontal Segment Sweep). At the same time, the vertical deflection signal must move the beam to one of four register locations (Vertical Staircase Generator); within that location start the beam at a specific point (Vertical Dot Generator); and move the beam vertically from that point (Vertical Segment Sweep).

The deflection amplifiers must take these fast, complex signals and amplify them linearly to the level necessary for CRT deflection. The deflection amplifiers are class A, push-pull, emitter coupled differential amplifiers with a gain of about 50.

The Horizontal and Vertical Deflection Amplifiers are identical. However, the horizontal input signal is somewhat greater than the vertical input signal because the display is wider (2") than it is high (1"). Since both amplifiers are alike, only the Horizontal Amplifiers will be discussed.

The input to Q1 in the Horizontal Deflection Amplifier (Figure 2-51) is the output of the horizontal channel emitter-follower. Assuming no input, the amplifier is in a static condition with Q1 biased on by the difference in voltage between Q1 emitter and the emitter load of the emitter-follower. With Q1 on, and in the center of its active region, current flow through R1 will make the collector some voltage less than -80 volts (about -65 volts), and the emitter some voltage less than +6 volts. Since Q1 emitter is connected through R5 to Q2 emitter and Q1 emitter is more negative than +6, the voltage on Q2 emitter from Q1 lowers current flow through Q2 and current flow through R3 will make the collector some negative voltage (about -25 volts), which, however, is less negative (more positive) than Q1 collector. Since the left hand deflection plate of the CRT is tied to Q1 collector and the right hand deflection plate tied to Q2 collector, the voltage difference between them will be about 40 volts, which is sufficient to position the beam close to the right hand plate (most positive).

Now assume a negative going deflection vol-

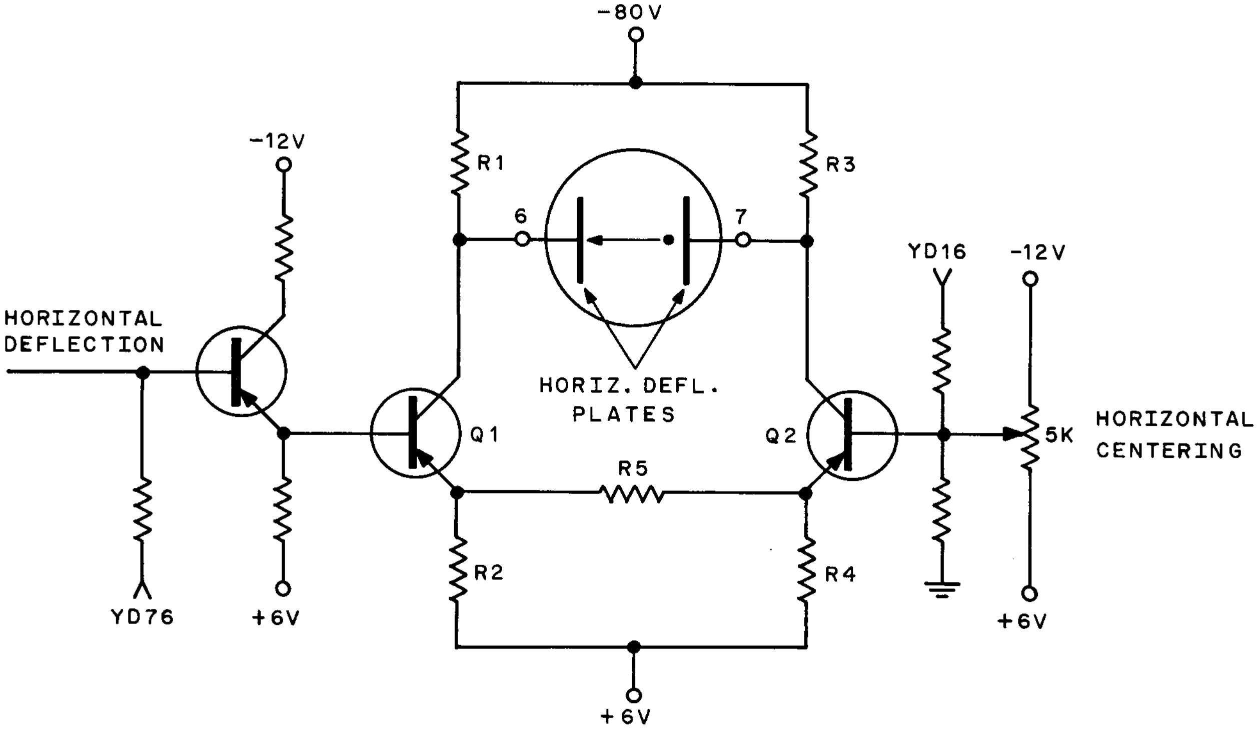


Figure 2-51. Horizontal Deflection Amplifier Schematic

tage at the output of the horizontal channel emitter follower. This negative going voltage is applied to the base of Q1 and increases collector current.

Collector current increase through R1 makes the collector of Q1 less negative (more positive) and the CRT beam moves to the left on the diagram. At the same time, increased Q1 current through R2 (Q1 emitter resistor) makes the voltage coupled to Q2 emitter through R5 more negative. This decreases emitter-base voltage of Q2 and Q2 collector current decreases. The decreased collector current through R3 (Q2 collector resistor) makes the collector of Q2 and the right hand plate of the CRT more negative, which, in effect, doubles the movement of the CRT beam caused by the left hand plate going positive. Thus, the circuit produces push-pull deflection. The CRT beam, then, will follow the input waveform applied to Q1 base, and Q2 will aid the effect, thus less input voltage is needed for a corresponding movement of the CRT beam than would be the case without Q2.

The potentiometer connected to the base of Q2 sets the static level of current through Q2 producing the IR drop across R3 and determines the effective voltage difference between the collectors of Q1 and Q2. This determines the starting position of the beam. Because the input to Q1 always varies in a negative direction, this makes the CRT beam move right to left from the starting position.

There is a logic input, designated YD76 (digit 7 offset), derived from the matrix that introduces a small increment of negative voltage when a digit 7 is displayed. This moves the whole digit 7 slightly left on the display for better readability and a more pleasing display.

Another logic input, designated YD16 (digit 1 offset), also derived from the matrix, introduces a small increment of negative voltage when a digit 1 is being displayed. This places the two segments comprising digit 1 (0 and 1 segments) slightly further to the right (or less to the left) than normal for these segments when used in another character. This again makes for a more readable and pleasing display.

The Vertical Deflection Amplifier (Figure 2-52) operates exactly as the Horizontal Deflection Amplifier. The 5K variable potentiometer in the base bias network of Q2 allows setting the static current of Q2. The starting point of the beam is toward the bottom plate. Display start is the rightmost digit (C1) of the lowest register (R1) (See Deflection Voltage Relationships diagram).

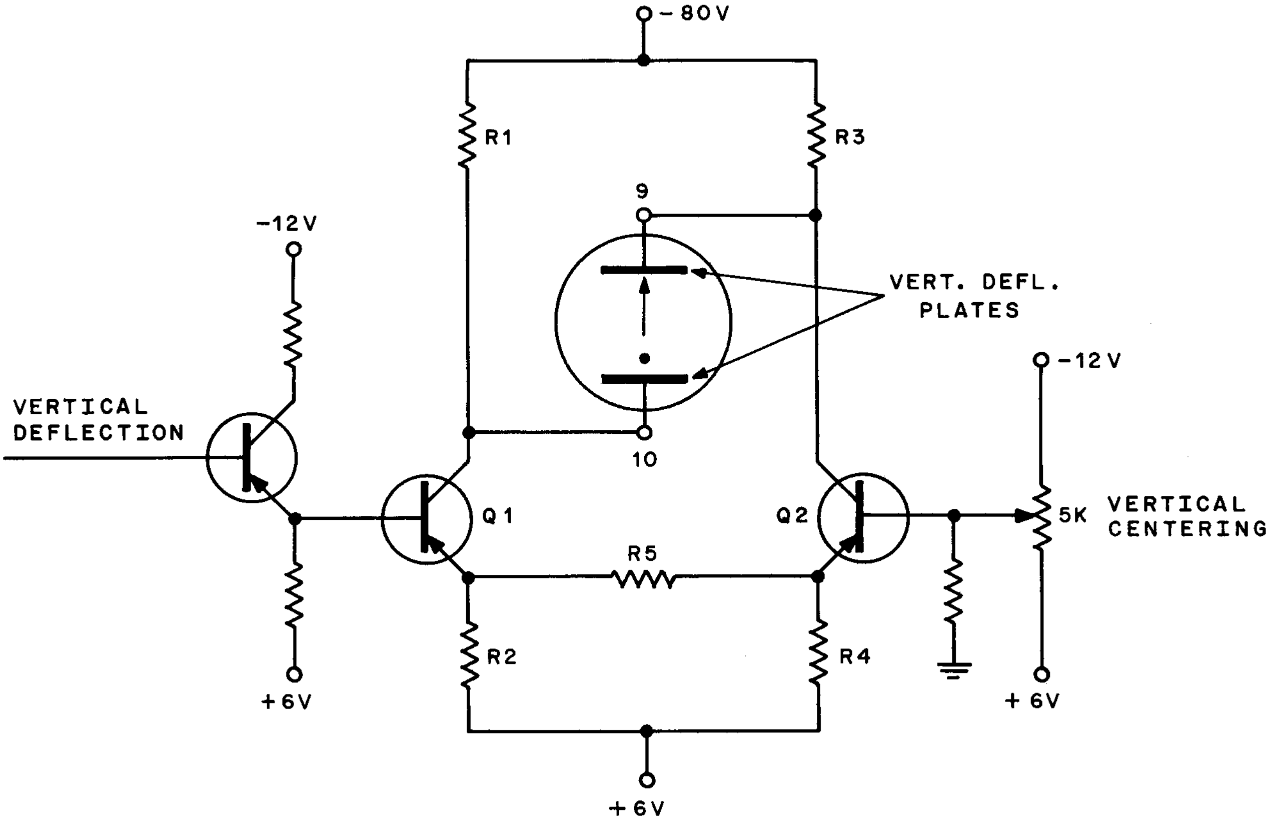


Figure 2-52. Vertical Deflection Amplifier Schematic

J. DISPLAY BLANKING

The intensification of the electron beam on the CRT is controlled by the Blanking circuits. The CRT is normally in a blanked condition and will be intensified (unblanked) by the action of the blanking logic.

1. UNBLANKING INVERTER

The unblanking of the CRT is accomplished by an inverter on the power supply card (PWX) whose output is capacitively coupled to the CRT grid. (See Figure 2-53.) The CRT grid is normally biased to cut-off with respect to the CRT cathode by an amount determined by the setting of the INTENSITY Control. The input to this inverter is the output of a Common OR Gate (COG), designated YBL5. I-200, I-203 and I-204 are connected as a Common OR Gate (COG) by a collector load resistor which is common to all three inverters.

Operation of the PWX inverter causes unblanking of the CRT. The collector load resistor forms part of a voltage divider between -80 volts and ground. The PWX board inverter is biased off by the base voltage divider. Thus, the collector voltage is about -40 volts due to the voltage divider in the collector circuit. C, then, is -40 volts on the collector side. When the inverter turns on, ground effectively appears at the collector. A change of -40 to ground (0V) is a positive transition, and the 40 volt positive transition is coupled through C to the grid of the CRT, and unblanks the CRT.

The PWX board inverter turn-on is controlled by a three inverter OR gate (O-500) with a common collector load resistor, which acts as a negative AND. If all three inverters are off, then the input (YBL5) to the base of the PWX inverter is -12 volts, and the inverter turns on, which provides unblanking for the CRT. If any one of the inverters is on, then the input to the base of the PWX inverter is 0 volts, the inverter turns off, and the CRT is blanked.

a. TRAILING EDGE BLANKING. I-200 is controlled by O-199 acting as a -AND. If all inputs are False, which will be at B7 and B15 times for 3 μsec each time, then the output is False, I-200 is biased on and the CRT is kept blanked for this 3 μsec. At all times other than B7 or B15, one of O-199 inputs will be True, and I-200 biased off, which will permit unblanking if I-203 and I-204 are also off. Since each segment is 24 μsec long (2 per each 16 Bit times, see Segment Generator discussion) this blanking by I-200 keeps the CRT blanked for 3 μsec at the end of each segment time. During this time the segment sweep is being completed and the segment waveform returning to zero, thus retrace blanking is controlled by I-200.

b. LEADING EDGE BLANKING. I-203, controlled by O-202 acting as a -AND, acts exactly the same as I-200 for 3 μsec during each B0 and B8 time. This blanks the leading edge of each segment for 3 μsec. Therefore, segment unblanking can occur at the CRT for 18 usec during the 24 μsec segment sweep time by the action of I-200 and I-203, provided that I-204 is off.

c. SEGMENT UNBLANKING. For CRT unblanking YBMX3 at O-500 must be False. For YBMX3 to be False, I-204 input must be True. I-204 is controlled by A-250 (Figure 2-53). If all inputs to A-250 are True (0 V) then the output is True, I-204 is biased off, and YBMX3 is False. PSZ3 will be True when, and only when, EPC is zero. Thus unblanking cannot occur if EPC is NOT zero, meaning that the machine is performing a function. YBMS3 will be True at A-250 through O-201 when a minus sign is to be displayed in C1 time. At all other times (C2 through C14) A-250 will be enabled because Display Control FF is set, and set output, YYC1 True, is applied through O-021 to A-250 (AR1).

The matrix outputs will be True at A-250 for each specific segment to be displayed (unblanked). The development of the matrix signal will be covered under Matrix discussion.

2. DIODE MATRIX

The Diode Matrix (Figure 2-54) decodes the setting of D Counter in a manner that permits the digit represented by the setting of D Counter to be displayed as a character on the CRT. In addition, the matrix enables modifying certain characters such as a 3, and provides deflection modifications such as digit 7 and digit 1 offset signals.

a. BASIC CHARACTER. The basic character from which all other characters are formed is a figure eight (8). The other nine digits are formed by NOT unblanking the undesired segments. While there are 12 segments produced for each character, some are never used, that is, they are never unblanked.

b. CHARACTER COUNTER. The timing of the twelve (12) segments is derived from a character counter composed of D, E, F, and G FF's in the timing chain. This group of FF's cycles every 288 μsec, which is one column time. At R1 time all of these FF's are reset (see Truth Table) and each of the 12 segments is numbered binarily from this starting time.

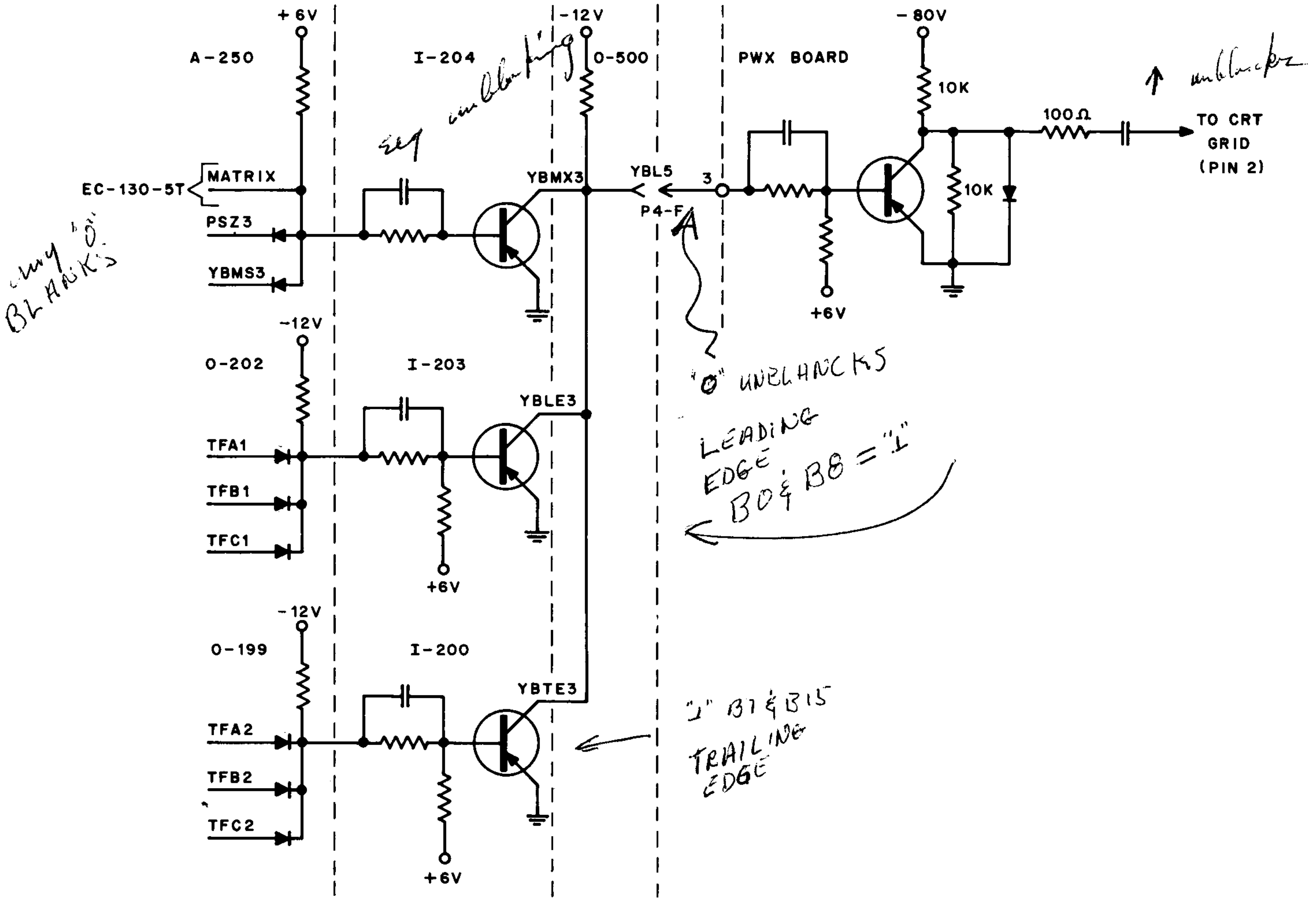
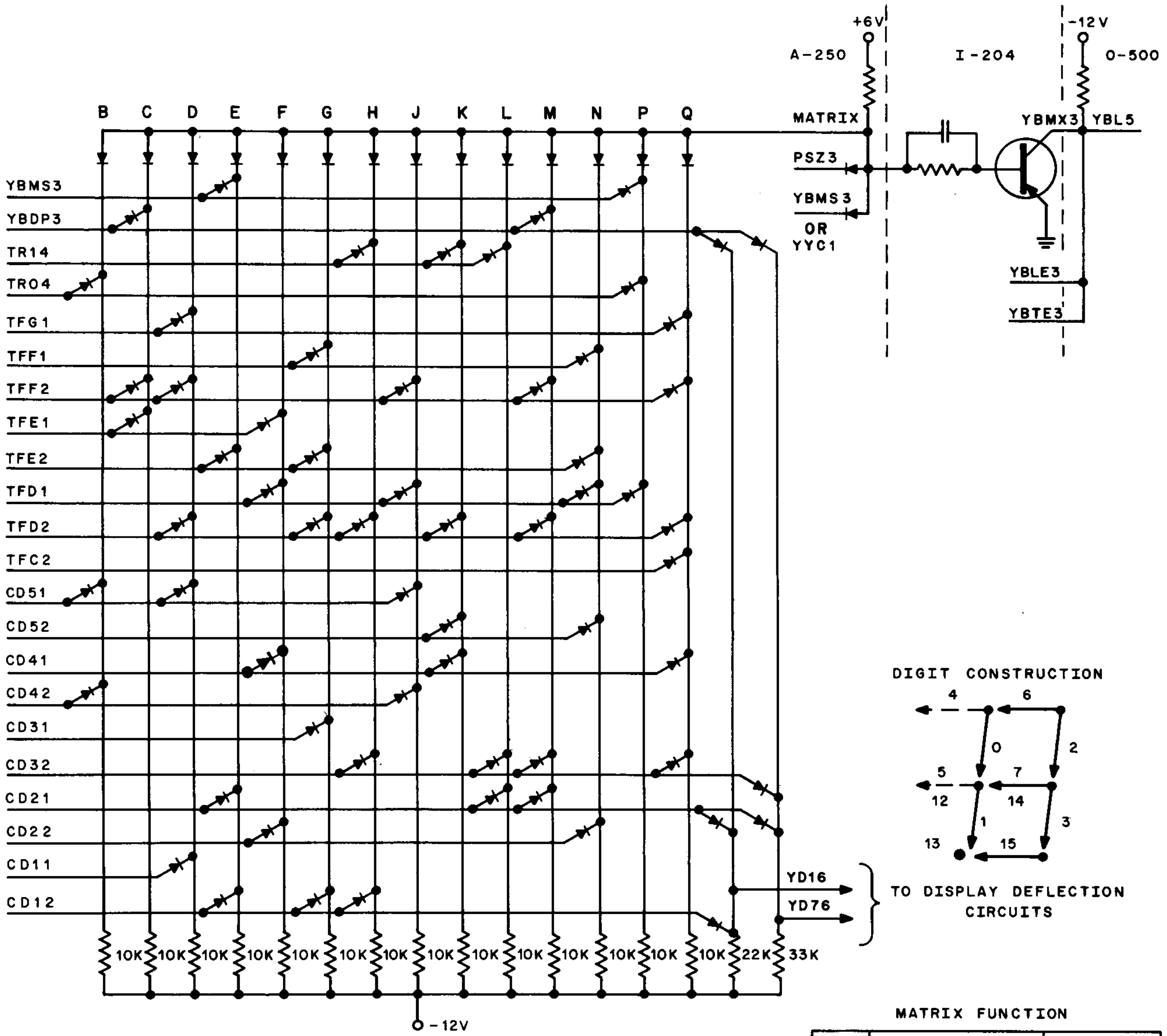


Figure 2-53. Unblanking Inverter Logic

c. BASIC MATRIX OPERATION. Basically, the matrix consists of OR gates controlling an AND gate. In the Matrix Logic diagram (Figure 2-55) all of the OR gates must have at least one True input for the AND gate (A-250) to have a True output. A-250 True output permits CRT unblanking for the 24 μsec of a segment sweep. The output of the OR gate (O-500) fed by A-250 is modified by the action of I-203 and I-200, which prevents unblanking for 6 μsec of the 24 μsec available through segment unblanking. This prevents the leading and trailing edge of the segment waveform from being unblanked, and provides total unblanking of 18 μsec for each segment.

The inputs to A-250 are designated as bus B, C, etc. and are similarly labeled on the matrix schematic (See Figure 2-54). One input only to each of the OR gates that control the busses needs to be True in order that the bus input to A-250 be True. When all inputs to A-250 are True, which means all busses are True, then A-250 output is True.

In summary, Matrix decoding is done by qualifying OR gates that control an AND gate. If all inputs to the AND gate (A-250) are True at a specific segment time, then a 24 μsec True output from the AND gate, modified to 18 μsec by the action of "leading" edge and "trailing" edge inverters (I-203, I-200) at a common OR gate (COG), will cause an unblanking pulse of 18 μsec at the CRT grid, and that segment will be drawn.



MATRIX FUNCTION

BUS	BLOCKS SEG	AFFECTS DIGIT
B	14,15	4
C	4,5,12,13	D.P.
D	7	0
E	2,3,6,7,14,15	1
F	0	2,3
G	3	1,2
H	1	3,4,5
J	6	4
K	1	9
L	0,1	7
M	7,15	7
N	2	5,6
P	14	-SIGN
Q	7	MOD.3

CHARACTER COUNTER TRUTH TABLE

	TIMING FF'S				
SEG	D	E	F	G	REG
0	0	0	0	0	R1
1	1	0	0	0	R1
2	0	1	0	0	R2
3	1	1	0	0	R2
4	0	0	1	0	R3
5	1	0	1	0	R3
6	0	1	1	0	R4
7	1	1	1	0	R4
12	0	0	1	1	RS
13	1	0	1	1	RS
14	0	1	1	1	RO
15	1	1	1	1	RO

D COUNTER TRUTH TABLE

NO.	D1	D2	D3	D4	D5
0	0	0	0	0	0
1	1	0	0	0	0
2	1	1	0	0	0
3	1	1	1	0	0
4	1	1	1	1	0
5	1	1	1	1	1
6	0	1	1	1	1
7	0	0	1	1	1
8	0	0	0	1	1
9	0	0	0	0	1

Figure 2-54. Diode Matrix Schematic

d. MATRIX OPERATION ANALYSIS. One method of analyzing the action of the matrix is to assume a particular digit in D Counter, then determine what segments must be unblanked for that character, and then to qualify each bus, in turn, as True for these segments.

(1) Digit 8 Unblanking. Assume a digit 8 in D Counter. Reference to the Truth Table for D Counter shows D4, D5 set and D1, D2, D3 reset. Those outputs from D Counter, then, are True, and will be True for a complete segment pass of 12 segments. Reference to the Character Formation Diagram shows that to display a character 8 segments 0, 1, 2, 3, 6, 7, and 15 must be unblanked, therefore the busses controlling those segments must be True during those segment times.

Reference to the Matrix Function Chart shows that segment 0 is blanked by bus F, therefore, to be unblanked bus F must be True. Reference to the logic diagram shows that CD41 is an input to O-237, and CD41 is True when a digit 8 is in D Counter (D4 set). Therefore bus F is qualified. Segment 1 is controlled by bus H. Bus H OR gate (O-239) has an input CD12 which will be True when a digit 8 is in D Counter (D1 reset). Therefore, Bus H is qualified. Segment 2 is controlled by both bus N and bus E. Obviously some busses are multipurpose and operate to unblank similar segments used in several numbers. However, choosing N bus to qualify segment 2, O-248 has as an input CD22 which will be True when a digit 8 is in D Counter (D2 reset), therefore bus N is qualified.

By using the same procedure, each segment in turn can be qualified by D Counter input at certain of the busses. However, not all busses are qualified by D Counter, and must be qualified in some other manner. The character counter (D, E, F, and G FF) inputs qualify certain of the busses for the segment times, while the D Counter inputs qualify busses for the whole column time (288 usec). Reference to the Truth Table for the character counter shows that, for segments 0 and 1, E-F and G FF's are reset, therefore the reset outputs are True and can be used to qualify busses. Also, since R1 time delineates this reset condition of the FF's, R1 time developed by logic gates could also be used, and sometimes is.

The net result of D Counter inputs is to qualify busses D (CD51), E (CD12), F (CD22), G (CD12), H (CD12), B (CD51), J (CD51), K (CD41), L (CD32), M (CD32), N (CD12), and Q (CD32). Note that there can be more than one qualifying signal on a bus, but any one True signal qualifies the bus. This leaves only busses P and C to be qualified for the specific segments that make up character 8. TRO4 at O-249 (bus P) will be True for segments 0 through 13 which qualifies bus P for these segments. TFD1 (True) at O-249 qualifies bus P for segment 15, thus bus P is qualified for all segments except segment 14. TFF2 (True) at O-234 qualifies bus C for segments 0-1-2-3 and TFE1 True qualifies bus C for segments 2-3-6-7-14-15, thus bus C is qualified for segments 0-1-2-3-6-7-14-15. The combination of bus P and bus C disqualifies A-250, which was qualified for all segments by D Counter settings on the other busses, for segments 4-5-12-14, and thus busses P and C qualify A-250 for segments 0-1-2-3-6-7 and 15. Therefore, those segments will be drawn and a character 8 displayed.

(2) Digit 1 Unblanking. For another example, assume a digit 1 in D Counter, D1 will be set, all other D FF's reset. Bus D is qualified by CD11; bus F by CD22; bus H by CD32; bus B by CD42; bus J by CD42, bus K by CD52; bus L by CD32; bus M by CD32; bus N by CD52 and CD22; and bus Q by CD32. This leaves busses E, G, P, and C to be qualified for segment times. Since only segments 0 and 1 are displayed for a character 1, A-250 must be qualified only for those segments. Bus E is qualified for segments 0 and 1 by TFE2. Bus G is qualified by TFE2. Bus P is qualified by TRO4 for all segments except 14 and 15. Bus C is qualified by TFF2 for segments 0-1-2-3. Thus, busses E and G limit the unblanking to segments 0 and 1, which is the requirement for a character 1.

e. DIGIT 1 OFFSET. With reference to a character 1, the matrix provides a deflection modification signal that applied in the deflection circuits will place a character 1 slightly to the right of where these segments would be drawn when a part of another character. Note O-245, CD12 and CD21 will both be False only when a digit 1 is in D Counter. YBDP3 is False except when decimal point display is desired. Thus the output of O-245 is False when a digit 1 (segments 0 and 1) is to be displayed. When O-245 output is False, all diodes on YD16 bus are back-biased. The voltage on YD16, then, is proportioned by a voltage divider consisting of 22 K to -12 V, and 10 K and 47 K to ground at the Horizontal Centering Potentiometer. This applies a negative voltage increment to the normal voltage at this point and, in effect, removes a portion of left deflection, which effectively moves segments 0 and 1 to the right when they are displayed as a

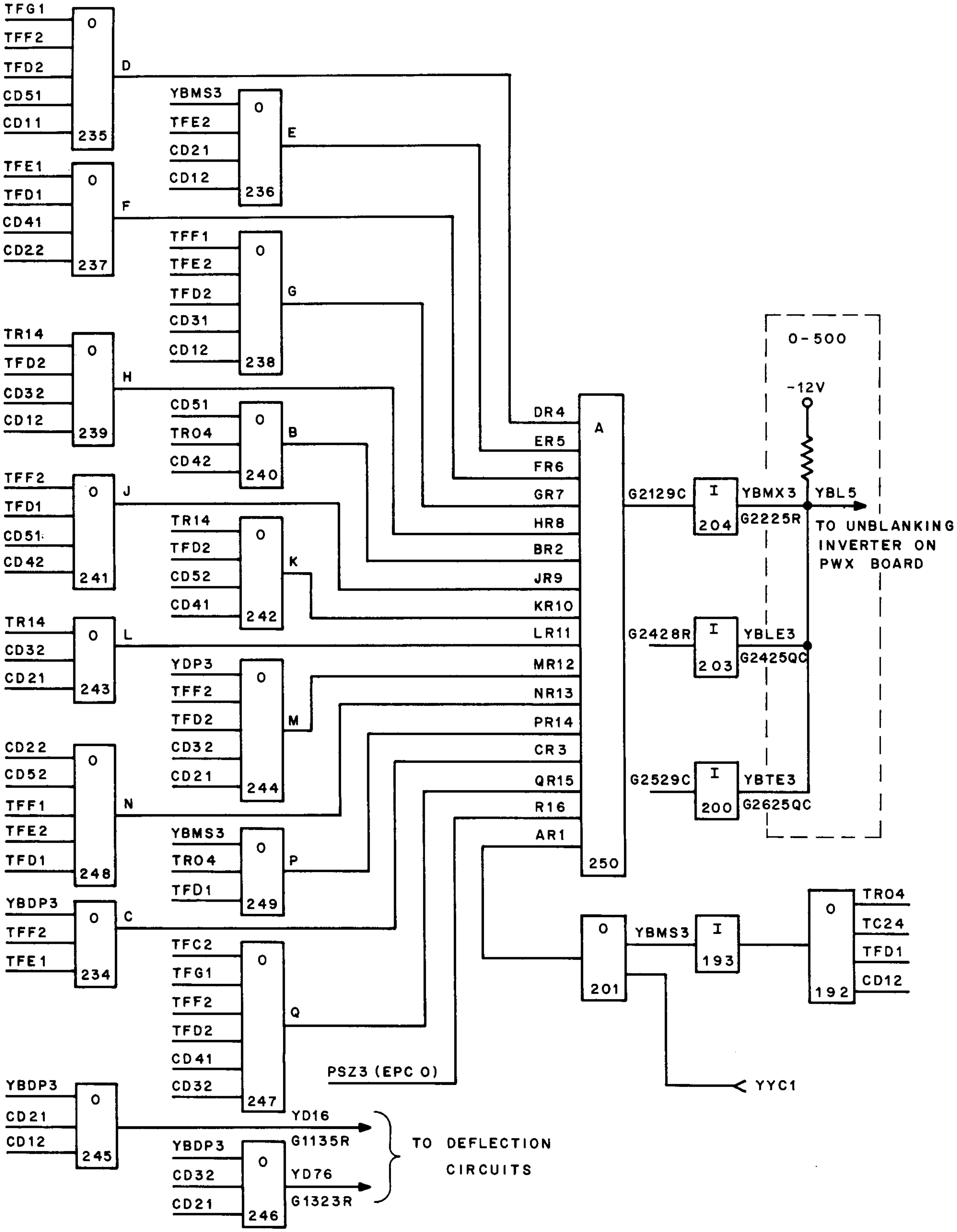


Figure 2-55. Matrix Logic

digit 1. At any time other than a digit 1, one of the inputs to O-245 is True and the output is True, which forward biases the diodes on bus YD76, and there is no offset voltage from this bus.

f. DIGIT 7 OFFSET. With reference to a character seven, the matrix provides an increment of negative voltage for extra left-deflection when a digit 7 is displayed, which will space a digit 7 slightly to the left of its normal position. This makes for a more pleasing and readable display. The output of O-246 will be True except when a digit 7 is in D Counter, when O-246 output will be False. When O-246 output is False, all diodes on YD76 bus are back-biased. The voltage on YD76, then, is proportioned by a voltage divider consisting of 33 K to -12 V, and 10 K at the input to the horizontal deflection emitter-follower. This applies a negative increment to the horizontal sweep voltage at this point and, in effect, adds a portion of left deflection, which offsets digit 7 to the left. When any input to O-246 is True, the output is True, which forward-biases the diodes on bus YD76, and there is no offset voltage from this bus.

g. MINUS SIGN UNBLANKING. Gate O-192 controls minus sign unblanking. TC24 False specifies C2 time, which is when the C1 minus sign data is in D Counter. If a minus sign is specified, there is one (1) data pulse in D Counter, thus D1 is set, and CD12 (D1 reset) will be False at O-192. TRO4 False and TFD1 False specify segment 14 (See Character Counter Truth Table). O-192 False output is inverted True by I-193, designated YBMS3. YBMS3 True is applied to qualify busses E and M for segment 14, which is used for minus sign display. Busses D and Q are qualified by TFG1, which is True for R1 through R4 time (total display time). Bus F is qualified for segment 14 by TFE1; bus G is qualified by TFF1; bus H by TFD2; bus B by CD42, bus J by TFF2; bus K by TR14; bus L by TR14; bus M by TFF2; bus N by TFE2; bus P by TFD1; and bus C by TFF2 and TR14. Therefore all busses are qualified for segment 14 time, and a minus sign will be displayed.

h. DECIMAL POINT UNBLANKING. Displaying Decimal Point means to unblank the CRT at segment 13 time. YBDP3 will be True when Decimal Point Logic, which is covered separately, specifies display. YBDP3 qualifies busses M and C for segment 13. Bus D is qualified by TFG1 and TFD2; bus E by TFE2; bus F by TFD1, bus G by TFF1 and TFE2; bus H by TR14; bus B by TRO4; bus J by TFD1; bus K by TR14; bus L by TR14; bus M by YBDP3; bus N by TFF1; bus P by TFD1, bus C by YBDP3; and bus Q by TFG1. Thus segment 13 is unblanked and Decimal Point will appear on the display.

YBDP3 is applied to YD16 bus and YD76 bus to eliminate the offset voltage to the deflection amplifier. This prevents the D.P. from being offset when displayed adjacent to a seven or one, as in .7 or .1.

K. DISPLAY TIMING AND LOGIC

Display occurs in the EC-130 only during Idle because only during Idle will PSZ3 (EPC0) be True, and PSZ3 is an enable input to A-225 in the compare logic. (See Figure 2-56.) Further, display can occur only for R1, R2, R3, and R4, which are called the display registers, because of TFG2 as an enable input at A-225 in the display logic.

1. DISPLAY TIMING

The basic timing for display is developed by M and N FF's. P FF permutes M and N FF's from a scale of 4 to a scale of 5. Effectively, then, one of the registers (R1) is displayed twice in the display cycle and is intensified on the CRT. This is desirable because R1 is the "answer" register.

a. COMPARE. The Compare Signal is developed to specify in the logic the time that a specific register is to be displayed, and the end of compare signal specifies the time that that register data is shifted to D Counter for matrix decoding. In the compare logic, M and N FF outputs are used to specify the register time and E and F FF outputs are used to designate time in D Counter for that register data. (See Figure 2-56.)

The basic compare signal is developed by A-225, whose output, inverted by I-226 and I-227, gives specific logic polarities where needed. When all inputs to A-225 are True, the output is True. TFG2 will be True at A-225 during R1 through R4 time and limits display to these registers. PSZ3 will be True at A-225 when EPC is zero, which limits display to Idle condition, that is, no function being performed.

M and N FF's remain in a given register state for one word time (data sequence), while E and F FF's cycle from R1 through R4 in each column time. Therefore, for a given word time, M and N specify the register to be displayed, and E and F FF's pick out that register time from each column time. Thus, it takes one word time to display each register, or a total of five (5) word times for a complete display cycle (R1 is displayed twice) and then the cycle starts over. In other words, YCPR3 will be True for one given register for each column time in one word time.

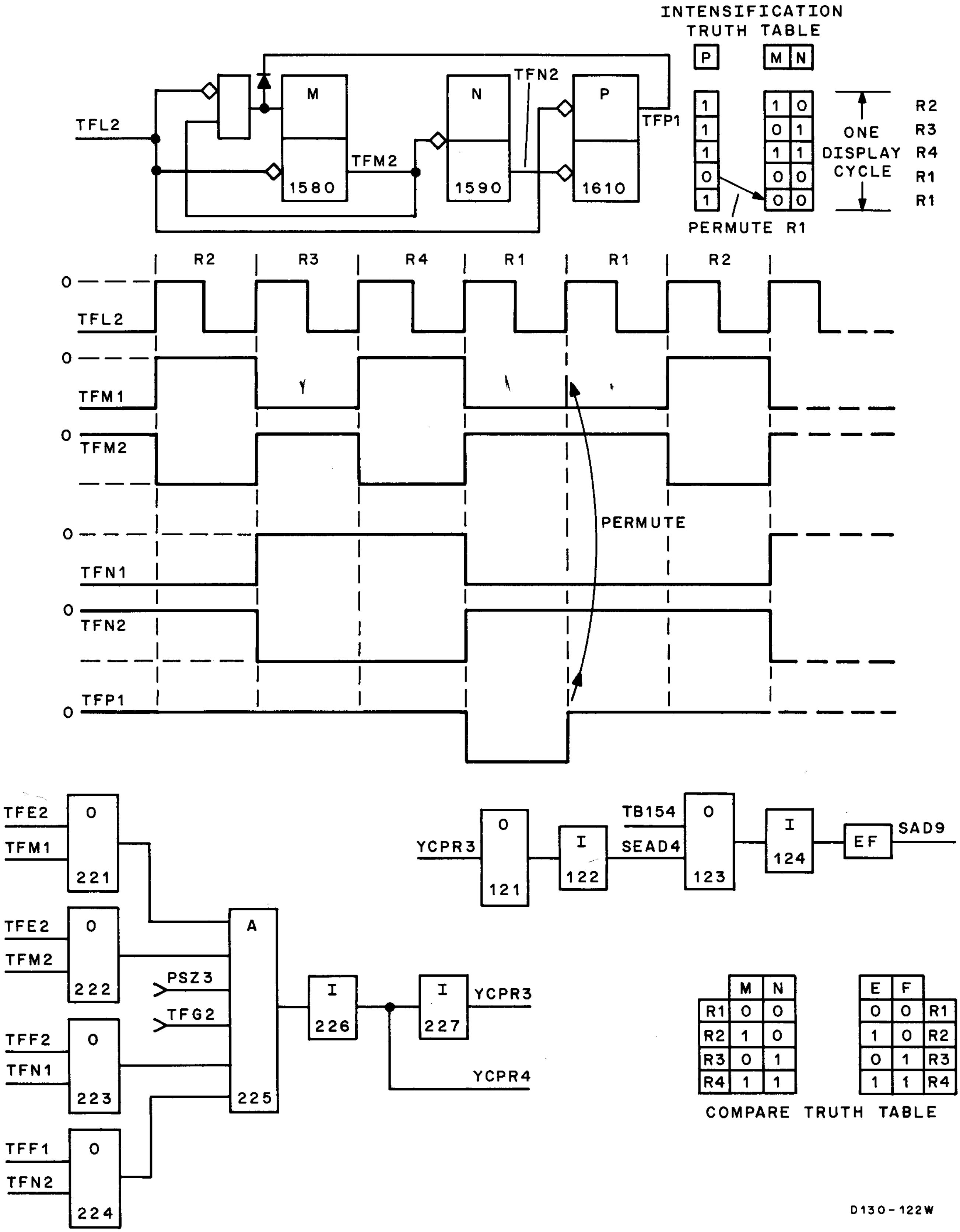
TFE2 and TFF2 are True during R1 time (See Truth Table), therefore gates O-221 and O-223 will have a True output at A-225 for R1 time. TFM2 and TFN2 are True during R1 time (See Truth Table), therefore O-222 and O-224 will have a True output at A-225 for R1 time. Thus, during R1 time, all inputs to A-225 are True and output of A-225 will be True. A-225 True is inverted False by I-226, designated YCPR4. YCPR4 False is inverted True by I-227, designated YCPR3.

TFE1 and TFF2 are True during R2 time (See Truth Table), therefore gates O-222 and O-223 will have a True output at A-225 for R2 time. TFM1 and TFN2 are True during R2 time (See Truth Table), therefore gates O-221 and O-224 will have a True output at A-225 during R2 time. Thus, during R2 time all inputs to A-225 are True and output of A-225 will be True. By use of the Truth Table and logic diagram, the derivation of Compare signal for R3 and R4 times can be found.

YCPR3 goes True at the end of the specific register to be displayed and YCPR3 signal is used to copy A Counter data into D Counter (Shift A to D) at the end of that specific R time. The data then remains in D Counter for one column time, then YCPR3 goes True for the same register in the next column and replaces D Counter data with new data. While the data is in D Counter, the matrix decodes this data and a character is displayed (See Matrix discussion). The Shift A to D is controlled by YCPR3 at O-121 in the machine logic. When YCPR3 goes True, the output of O-121 goes True and is inverted False by I-122, designated SEAD4. SEAD4 False enables O-123. When TB154 goes False, O-123 output goes False and, inverted True by I-124, is applied as SAD9 to the counter circuits to initiate a shift of A Counter data to D Counter. At the same time that the data setting of A is shifted A to D, A Counter setting is also shifted A to B, which preserves the data in the data sequence.

b. REGISTER 1 INTENSIFICATION. R1 is the answer register and is intensified (Brightened) in respect to the other registers by being shown twice in each display cycle. Since M and N FF's specify the register to be displayed, R1 is intensified by permuting (holding) M and N FF in R1 display time for an extra word time.

The permuting of M FF is accomplished by P FF set output applied through an isolating diode to the set input at M FF. (See Figure 2-56.) Assume all FF's reset. TFL2 True sets M and P FF's with N FF remaining reset. The Truth Table shows that this is the setting for R2. The next TFL2 resets M, which sets N (P remains set). This is the setting for R3. The next TFL2 True sets M, with N and P FF's remaining set. This is the setting for R4. The next TFL2 True resets M, which resets N, which resets P. This is the setting for R1. However, when P resets, TFP1 goes False, and the cathode of the isolating diode has -12 V applied. The next TFL2 ap-



INTENSIFICATION TRUTH TABLE

P	M	N		
1	1	0	ONE DISPLAY CYCLE	R2
1	0	1		R3
1	1	1		R4
0	0	0		R1
1	0	0		R1

PERMUTE R1

	M	N
R1	0	0
R2	1	0
R3	0	1
R4	1	1

E	F	
0	0	R1
1	0	R2
0	1	R3
1	1	R4

COMPARE TRUTH TABLE

Figure 2-56. Compare Signal Logic

plied to the AC gate at set input of M FF would normally set M FF because of the False to True transition from the AC gate. However, when the AC gate output goes True, the diode is now forward-biased and clamps the set input of M FF to -12 V, and M cannot set. Thus M and N FF's remain reset, which is R1 display time. Note, however, that the TFL2 True that fails to set M FF does set P FF. When P FF sets, TFP1 goes True (0 V) at the cathode of the diode, and the AC gate is able to set M FF when the next TFL2 transition occurs because the diode is effectively out of the circuit. Thus, after being held (permuted) in R1 display condition for one extra word time (data sequence), M and N FF's then cycle through R2, R3, R4, and R1, when the permute again occurs. In this manner R1 display is enabled twice in succession for each display cycle and is intensified on the display. The only function of P FF is for register intensification and P FF was formerly called "Intensity" FF.

2. DISPLAY LOGIC

Display Logic establishes character display time, Decimal Point position, and Minus Sign time, as well as incorporating the Matrix and Unblanking logic previously discussed. (See Figure 2-57.)

a. CHARACTER TIME. Characters are displayed in Registers 1 through 4 (R1 - R4) from C2 through C14 time. R1 through R4 time is specified by YYC1 True applied through O-201 to A-250 in the Blanking logic. YYC1 will be True if Display Control FF is set.

Display Control FF set and reset is controlled by AC gates on the set and reset inputs. TC23 is applied to enable the AC set gate, and TC153 is applied to enable the reset gate. YCPR4 True is applied as a positive transition to both AC gates. The first time YCPR4 goes True during C2 time, Display Control sets. Display Control remains set until the first time YCPR4 goes True in C15 time, when Display Control resets. Display Control set output, designated YYC1, is applied through O-201 to A-250 in the Blanking Logic. A-250 is enabled when YYC1 is True, which is when Display Control FF is set. Thus, YYC1 enables display unblanking from C2 time, when Display Control FF sets, until into C15 time, when Display Control FF resets. Therefore, unblanking is enabled from C2 through a part of C15 time. When Display Control resets, which is during C15 time, A-225 is inhibited by YYC1 False, and display unblanking is inhibited.

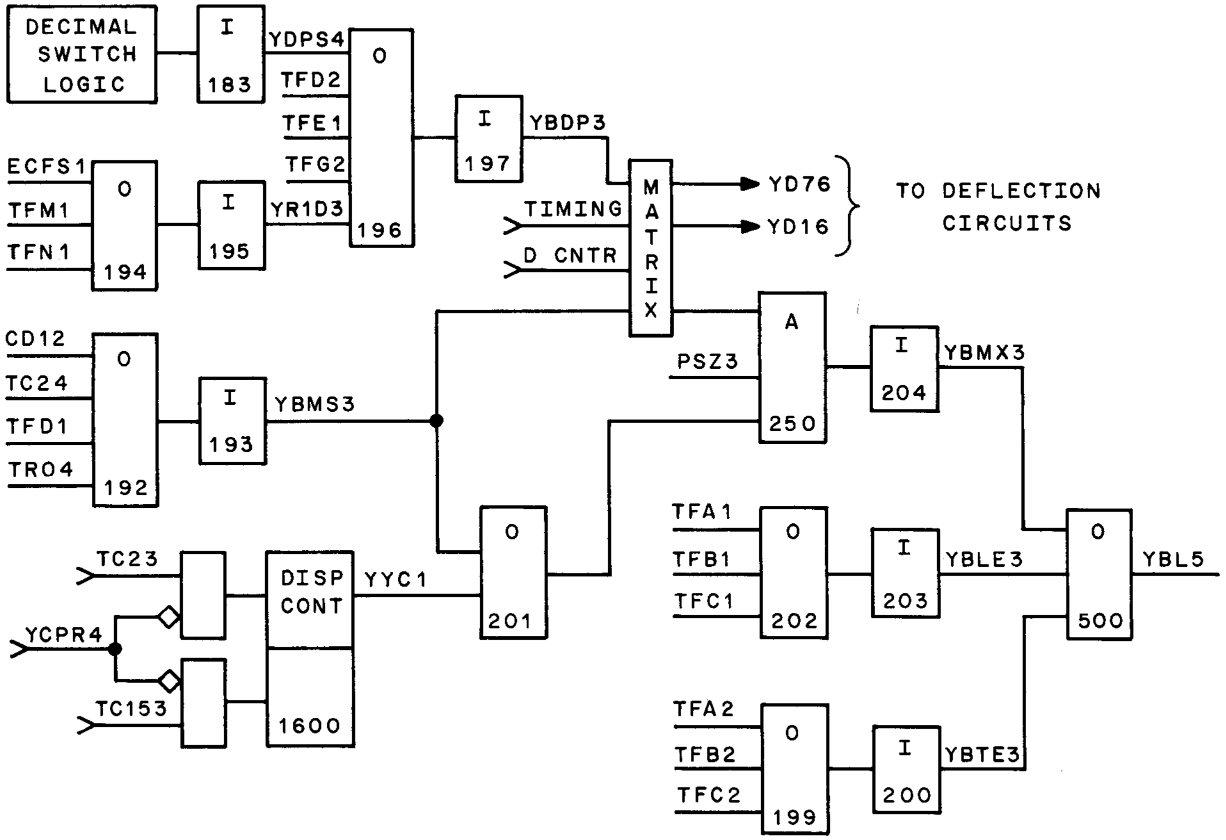


Figure 2-57. Display Logic

b. DECIMAL POINT LOGIC. The decimal point position logic specifies the column in which the decimal point will appear. YBDP3, which is the decimal point unblanking input to the Matrix, is developed by I-197 controlled by O-196. YBDP3 True enables decimal point unblanking, therefore the input to I-197 must be False for unblanking, and O-196 acts as a negative AND.

(1) Decimal Point Switch Logic. YDPS4 False at O-196 is developed by I-183 controlled by the Decimal Point Switch Logic. (See Figure 2-58.)

The input to I-183 is the output of A-182 and when A-182 inputs are all True, the output is True. The inputs to A-182 are a group of eight OR gates which have two (2) inputs each. All OR gate outputs must be True for A-182 output to to be True, however, only one input to each OR gate needs to be True for the output of that OR gate to be True.

The action of the decimal point switch is to provide a True input to four of the OR gates, which will make the output of those gates True. The action of H, J, K, and L FF outputs is to provide a True input to the other four OR gates at a specific column time. By the combined action of the decimal point switch and the FF outputs, the inputs to A-182 will be True only for one specific column time in each register.

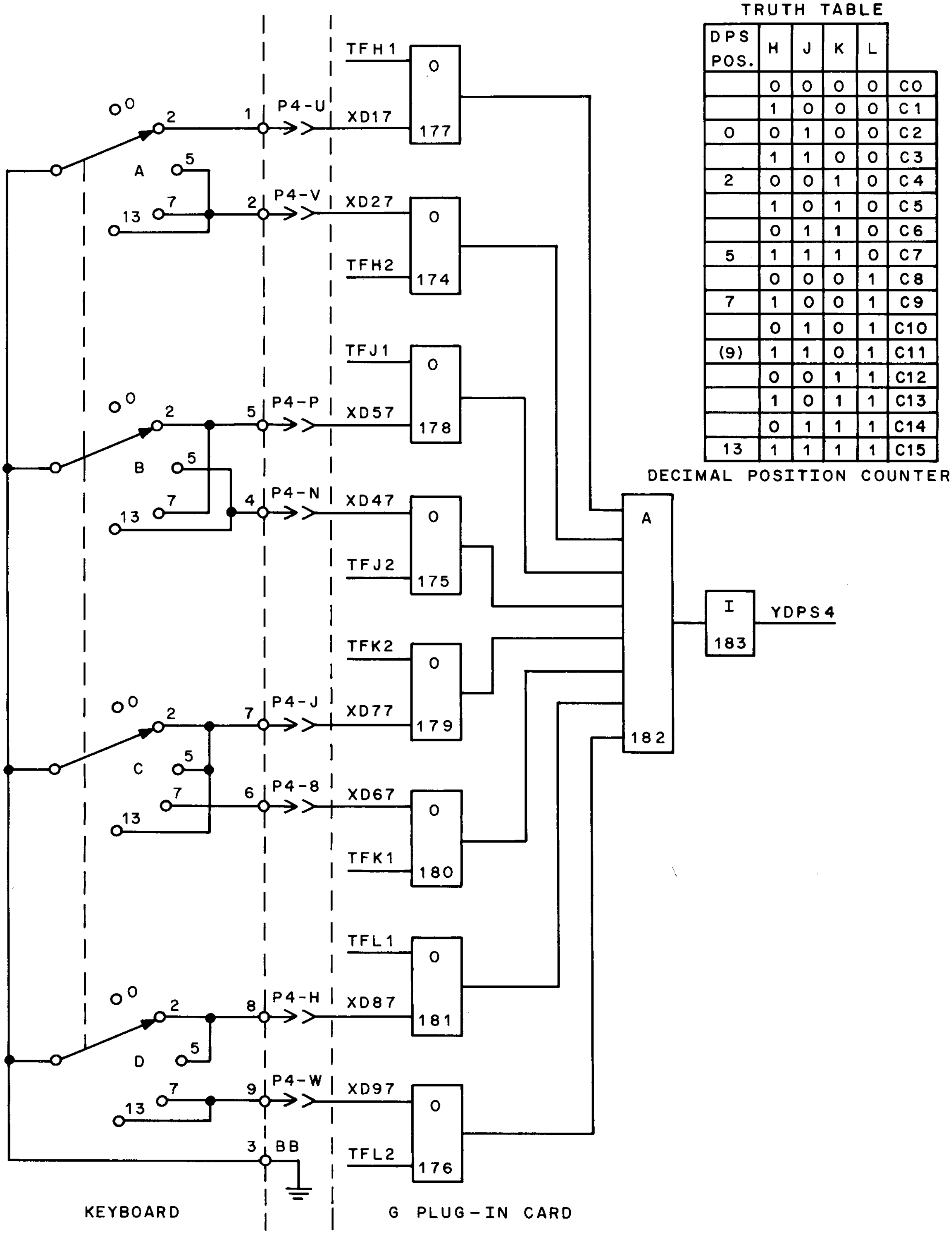
Assume decimal point switch on position 5. This specifies a decimal point in column 7 (C7). C7 is the time that C6 information is in D Counter for display decoding, and C6 is the column in which decimal point is displayed when 5 decimal places to the right of the decimal point is specified. Ground (True) is applied through active switch wafer connections to O-174, O-175, O-180, and O-181, which makes the output of these gates True at A-182. TFL2 at O-176 will be True for C7 time (See Truth Table), which makes the output of O-176 True at A-182 for C7 time. TFH1, TFJ1, and TFK1 True for C7 time make O-177, O-178, O-179 outputs True at A-182 for C7 time. Thus, all inputs to A-182 will be True for C7 time, and only for C7 time. Therefore, A-182 True output, inverted False by I-183, designated YDPS4, will enable O-196 for C7 time.

For another example, assume decimal point switch on 13, which specifies 13 digit spaces available to the right of the decimal point. Ground (True) is applied through active switch wafer connections to O-174, O-175, O-176, and O-179, which makes these gate outputs True at A-182. TFH1, TFJ1, TFK1, and TFL1 True for C15 time at O-177, O-178, O-180, and O-181, makes these gate outputs True at A-182. Thus all inputs to A-182 are True for C15 time, and only for C15 time. Therefore, A-182 True output inverted False by I-183, designated YDPS4, enables O-196 for C15 time, which is when C14 data is in D Counter for decoding.

By reference to the decimal point switch wafer connections and the Decimal Point Position Truth Table, the OR gate inputs necessary for True outputs at A-182 can be determined for each specific decimal point position. Note, however, that no decimal point display is permitted for switch position 0. Remembering that all inputs to A-182 must be True for decimal point display, O-175 output, for instance, will be False because of TFJ2 False input. Thus A-182 will be inhibited by O-175. Of course, at this time O-177 is False because of TFH1 False input; O-197 output is False because of TFK1 False input; and O-181 output is False because of TFL1 False input. However, any one of the gate outputs being False at A-182 inhibits decimal point display, so if more than one is False, it is of no consequence.

(2) Number Entry Decimal Point Blanking. YR1D3 input to O-196 will be False except during number entry, when the decimal point in R1 is kept blanked until the number is entered by the initiation of a function. YR1D3 is developed by I-195 controlled by O-194, which acts as a negative AND. TFM1 and TFN1 specify R1 display time, and will be False for R1 time. ECFS1 specifies a function, and will be False during a number entry. If all inputs to O-194 are False, and they will be False only during a number entry, the output of O-194 is False, and inverted True by I-195 acts to inhibit decimal point display for Register one (R1) only. During all other functions, ECFS1 will be True, thus YR1D3 will be False, and O-196 will be enabled for decimal point display.

(3) Decimal Point Unblanking. Decimal Point on the display is developed by unblanking segment 13. TFG2, TFD2, and TFE2 will be False at O-196 for segment 13 time only. (See Character Counter Truth Table - Display Blanking discussion.) Therefore, segment 13 is enabled to be unblanked by action of O-196. In summary, the decimal point switch position together with H, J, K, and L FF settings determines the column position



TRUTH TABLE

DPS POS.	H	J	K	L	
	0	0	0	0	C0
	1	0	0	0	C1
0	0	1	0	0	C2
	1	1	0	0	C3
2	0	0	1	0	C4
	1	0	1	0	C5
	0	1	1	0	C6
5	1	1	1	0	C7
	0	0	0	1	C8
7	1	0	0	1	C9
	0	1	0	1	C10
(9)	1	1	0	1	C11
	0	0	1	1	C12
	1	0	1	1	C13
	0	1	1	1	C14
13	1	1	1	1	C15

DECIMAL POSITION COUNTER

Figure 2-58. Decimal Point Switch Logic

of the decimal point; YR1D3 permits disabling decimal point display for R1 time during a number entry; and TFG2, TFD2, and TFE2 inputs to O-196 delineate segment 13, which is the decimal point display segment. O-196 acts as a negative AND, and when all inputs are False, the output of O-196 is False. O-196 False output, inverted True by I-197, designated YBDP3, is applied in the matrix to provide unblanking for segment 13.

c. MINUS SIGN. The Minus sign on the display is segment 14 drawn in the position of segment 7, with all other segments blanked. Minus sign logic signal designated YBMS3, is developed by I-193 controlled by O-192 acting as a negative AND. TRO4 and TFD1 inputs to O-192 are False for segment 14. TC24 will be False when C1 data, which specifies minus sign, is D Counter for decoding. CD12 will be False when a count of 1 is in D Counter, which specifies a minus sign in C1 time. When all inputs to O-192 are False, the output is False and inverted True by I-193, designated YBMS3, is applied in the matrix to unblank segment 14.

YBMS3 True is also applied directly through O-201 to enable A-250. This is necessary because A-250 is only enabled from part of C2 into part of C15 time by Display Control FF set output (YYC1). Minus sign display occurs before Display Control FF becomes set to enable character display.

L. POWER SUPPLIES

The power supply circuits in the EC-130 provide the operating voltages for machine function. The operating voltages are +6, -12, -80, and -2400 volts DC. While the +6 volts, -12 volts, and -80 volts are interconnected (Figure 2-59), electrically there are three distinct supplies and they are discussed separately. The -12 volt supply is mounted on the PDA board, and the other supplies are mounted on the PWX board.

1. +6 VOLT SUPPLY

The rectifier section of the 6 volt supply (Figure 2-60) is a conventional full-wave rectifier with capacitive input. With 14 volts (RMS) across each half of the transformer, the 2000 µfd input capacitor will charge to approximately 20 volts. (See Lesson 17 of FRIDEN Electronic Course.)

The base of the 2N669 transistor is held to approximately 6 volts by the action of the IN709A zener diode and the 470 ohm and 1K ohm resistors. Thus any change in the output 6 volts, which is taken from the emitter of the transistor, is immediately felt as a change of emitter to base voltage.

Assume an increase in the +6 volts output caused either by a change in load or a change of input AC. Since the base of the transistor is held fixed by the zener, then the emitter becomes more positive with respect to the base, and transistor current increases. This increase in current causes the IR drop across the 40 ohm series resistor to increase, which makes the emitter of the transistor less positive and lowers the output voltage toward +6 volts. The circuit components are chosen to provide 2% regulation, or better.

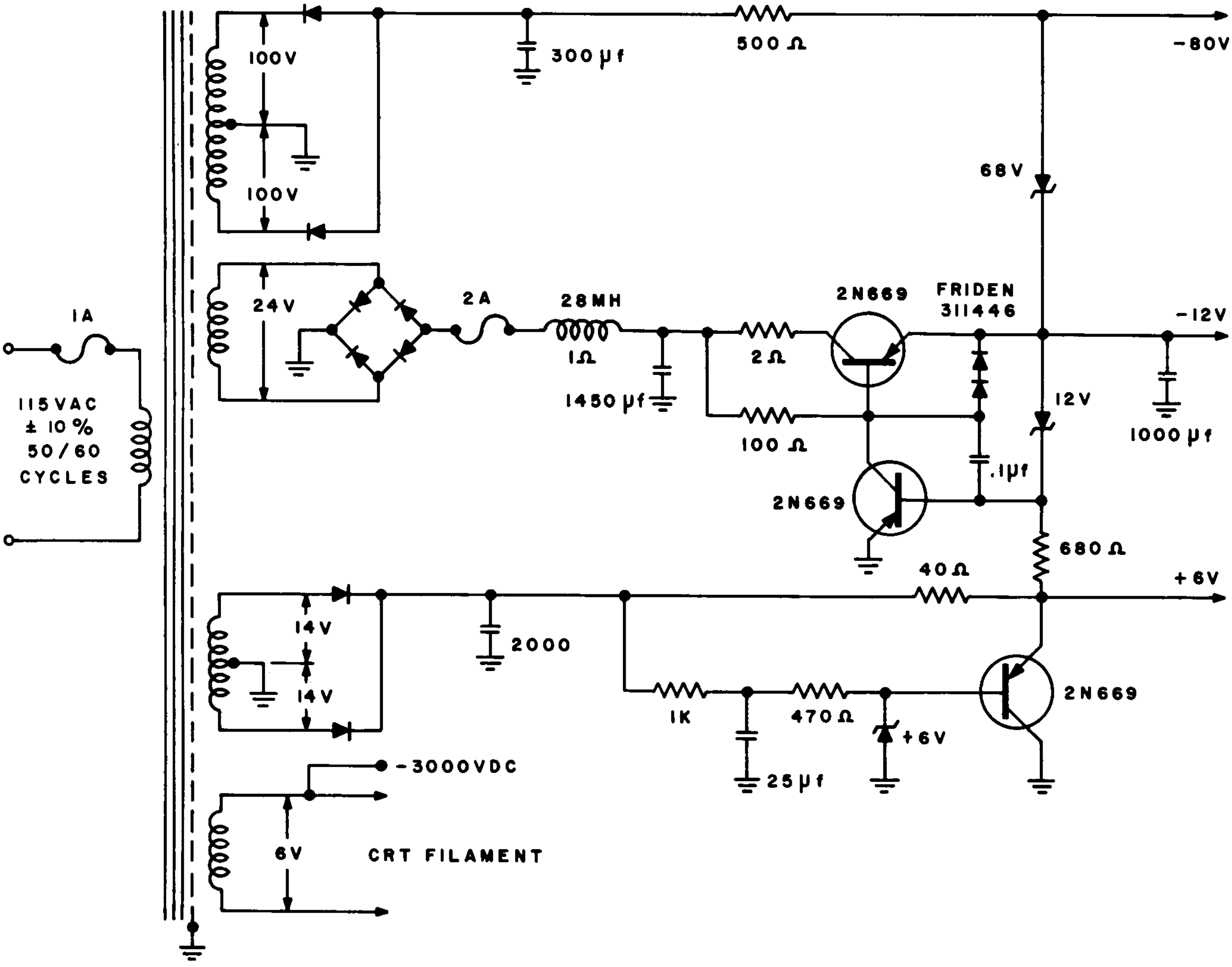


Figure 2-59. Power Supply Schematic

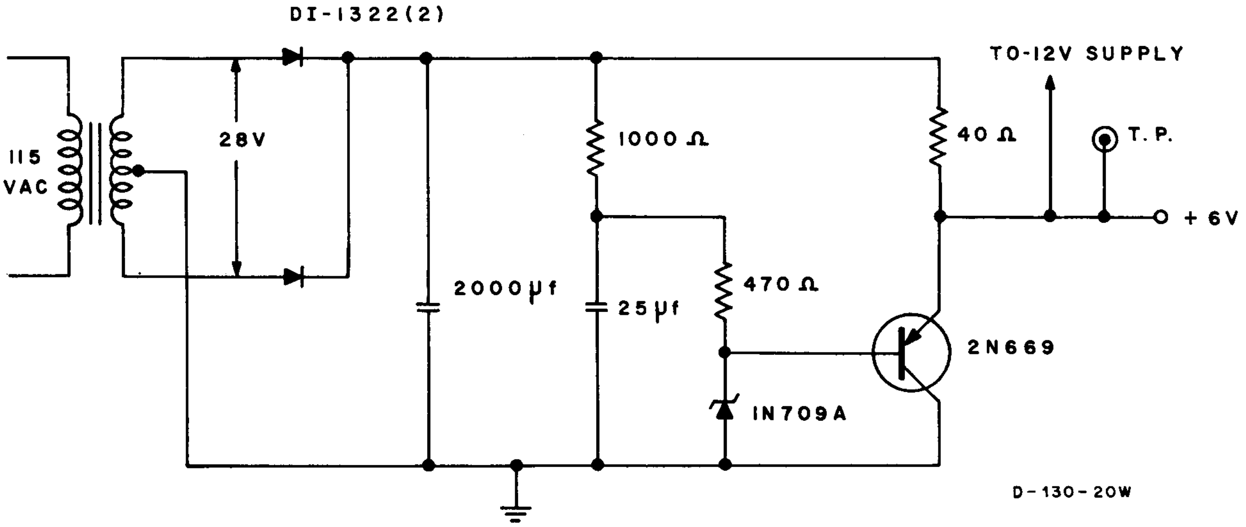


Figure 2-60. + 6 Volt Supply Schematic

The 25 µfd capacitor to ground between the 1000 ohm and 470 ohm resistor provides additional filtering to keep AC ripple to a minimum at the transistor base.

2. -12 VOLT SUPPLY

A functional schematic of the 12 volt supply is illustrated in Figure 2-61. The rectifier section is a conventional full-wave bridge circuit with a choke input. The voltage developed across the 1450 µf capacitor will be approximately -35 volts, neglecting the IR drop across the resistance of the filter choke.

This -35 volts is reduced to -12 volts at the output by the voltage drop across transistor Q2 in series with the 2 ohm resistor, and the -12 volts is regulated by the current flow through the transistor. The emitter of transistor Q2 is held constant by the IN759 zener diode to -12 volts. The base of transistor Q2 is biased by transistor Q1 in series with the 100 ohm resistor. The base of transistor Q1 is biased by the current flow through the 680 ohm resistor to the +6 volt supply.

Assume that the -12 volts rises, either because of an increase in AC input or a change in load, the IN759 zener current will lower and the voltage at the base of Q1 will become more positive because of the lower zener current through the 680 ohm resistor. This causes Q1 to conduct less heavily, which decreases the IR drop across the 100 ohm resistor. This, in turn, causes the base of Q2 to go in a negative direction, which increases current flow through transistor Q2 and through the 2 ohm resistor. The voltage dropped across these two in series increases, thus, the output voltage, which is the difference between this IR drop and the -35 volt output of the supply, goes less negative and compensates for the rise of the -12 volts. The circuit constants are chosen so that the voltage is regulated to 2% or better.

The two diodes between base and emitter of Q2 ensure that the voltage between these two points will never exceed 1 volt, which is protection for the transistor. The .1 µf capacitor allows fast voltage changes to appear at the base of Q2 for better regulation and also tends to prevent low frequency oscillations from developing.

3. -80 VOLT SUPPLY

A functional schematic of the -80 volt supply is as shown in Figure 2-62. The rectifier section is a conventional full-wave circuit with capacitive input. The voltage developed across the 300 µf input capacitor will be approximately 141 volts. This 141 volts is reduced to -68 volts in series with -12 volts from the regulated -12 volts supply by the zener diode current through the 500 ohm series regulating resistor.

Assume the -80 volts decreases, either because of less than 115 VAC input or an increase of load current. The zener will pass less current, thus less IR drop across the 500 ohm regulating resistor, and the output voltage will rise to a more negative value. While the -80 volt regulation is not quite as precise as the -12 or +6 volt supplies because of fewer components, the output regulation is satisfactorily held to 2% or better.

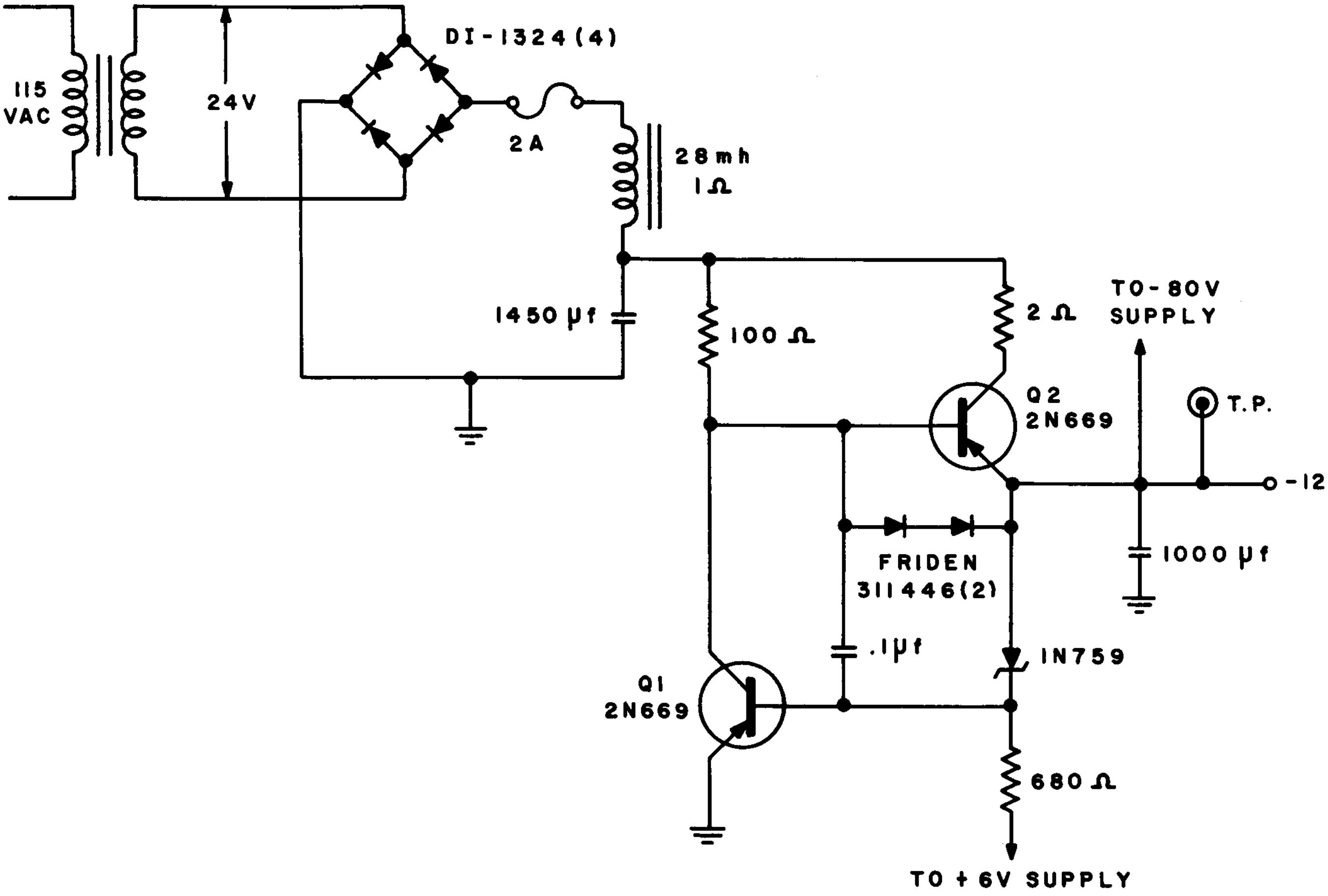


Figure 2-61. -12 Volt Supply Schematic

4. -2400 VOLT SUPPLY

The high voltage, -2400 volt DC, supply (Figure 2-63) in the EC-130 is a modified voltage multiplier circuit driven by a 2KC multivibrator instead of 60 cycle AC. This is sometimes called an "Oscillator" power supply. An advantage of this oscillator type of drive to the power transformer is that higher output voltage can be obtained from the same number of turns on the transformer because the rate of change of primary current at 2KC is higher than the rate of change at 60 cycles.

Voltage Multiplier circuits are adequately covered in the FRIDEN Electronic Course, Lesson 17, page 6. Therefore, only the modifications peculiar to the EC-130 such as the oscillator and the output connection of the transformer will be covered in this discussion.

a. OSCILLATOR. While the power transformer driver is called an oscillator, a more correct name is A-Stable multivibrator. Q1 and Q2 transistors are alternately turned on and off at a rate determined by the time constants of C1R1 and C2R2. The time constants are so chosen as to provide approximately 2KC output.

The output is taken from the emitter of Q2 and is used to drive Q3 through a base connection. The diode between Q3 base and ground is to ensure that the base never becomes more positive than about .5 volts. Q3 is a power transistor that conducts heavily when the base goes negative. Current then flows from -12 volts, through Q3, the transformer primary, and ground.

Q3 is practically a short circuit when conducting, therefore all of the -12 volts are across the primary of the transformer. In addition, when Q3 cuts off the sudden collapse of the current field of the primary provides an "inductive kick" that momentarily adds a further -12 volts, thus the total drive voltage across the transformer primary is 24 volts. In the secondary, the 24 volts is stepped up to approximately 400 volts.

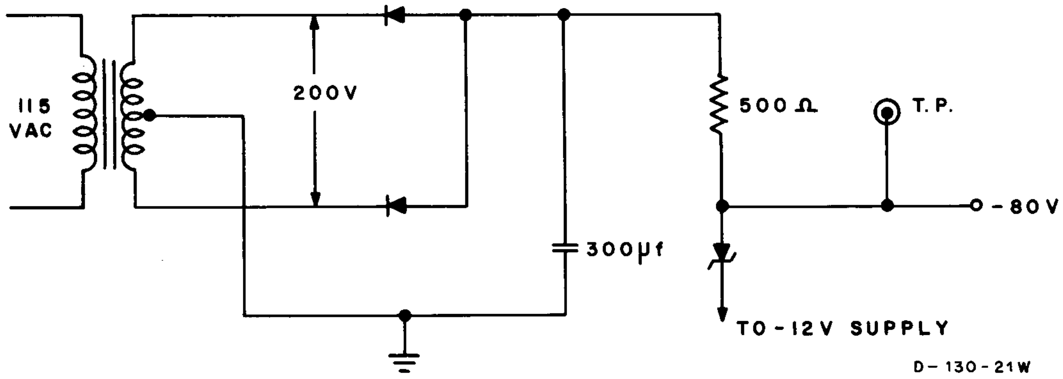


Figure 2-62. -80 Volt Supply Schematic

An RC filter consisting of 10 ohms and 100 µfd prevents the 2KC changes across the transformer primary from being fed-back into the -12 volt supply and appearing as an unacceptable level of 2KC ripple.

b. VOLTAGE MULTIPLIER. The power transformer is connected between the two multiplier sections so that each section need only develop -1200 volts, thus certain insulation and wiring problems are avoided at the cost of a slightly higher insulation value on the power transformer itself. The multiplier sections are series-aiding and the output is -2400 to the voltage divider which supplies the DC operating voltages to the CRT.

5. CRT VOLTAGES

The acceleration of the electrons in the "electron gun" section of the CRT is determined by the potential between the cathode and the focusing anodes. (See Lesson 15 of FRIDEN Electronic Course.) If the cathode is more negative than the focus-accelerating anodes, then the anodes are more positive than the cathode, and the electrons are accelerated. The grid in turn is connected to a more negative potential than the cathode and serves to control the number of electrons in the beam, thus the "intensity".

The -2400 volt output is connected to a voltage-divider which permits division of the voltage for proper CRT operation. The grid is connected at the most negative point on the divider, and the potential with respect to the cathode is varied by the wiper arm of a 500K potentiometer. This control is designated INTENSITY. The three NE-2 lamps insure that the voltage between grid and cathode does not exceed approximately 210 volts. A difference greater than this could cause arc-over in the CRT elements. Also connected to the grid is the blanking pulse from the blanking circuit. In normal operation the CRT is cut-off. The blanking pulse lifts the CRT out of cut-off for the period of the pulse. The diode across the 2.2 megohm resistor is for DC restoration. The .1 µf capacitor places the arm of the INTENSITY potentiometer at AC ground.

The FOCUS potentiometer connection is at a point less negative (more positive) than the cathode, thus a positive accelerating potential on the focus-accelerating anode. Varying this potentiometer varies the point at which the electron beam is narrowest, and when that point is at the screen of the CRT sharpest focus is obtained.

The ASTIGMATISM Control is connected to -80 volts. This anode of the electron gun is the most positive point in the electron gun. Varying this control affects the "roundness" of the beam at the CRT screen.

Adjustment of INTENSITY, FOCUS, and ASTIGMATISM controls is covered in Section 3 of this manual.

The .005 µfd capacitor at the cathode of the CRT is to place this point at AC ground. Note that the cathode potential is also applied to the filaments. This prevents cathode to filament arc-over, but places the filament winding of the power transformer at somewhere near -2400 volts DC with respect to ground.

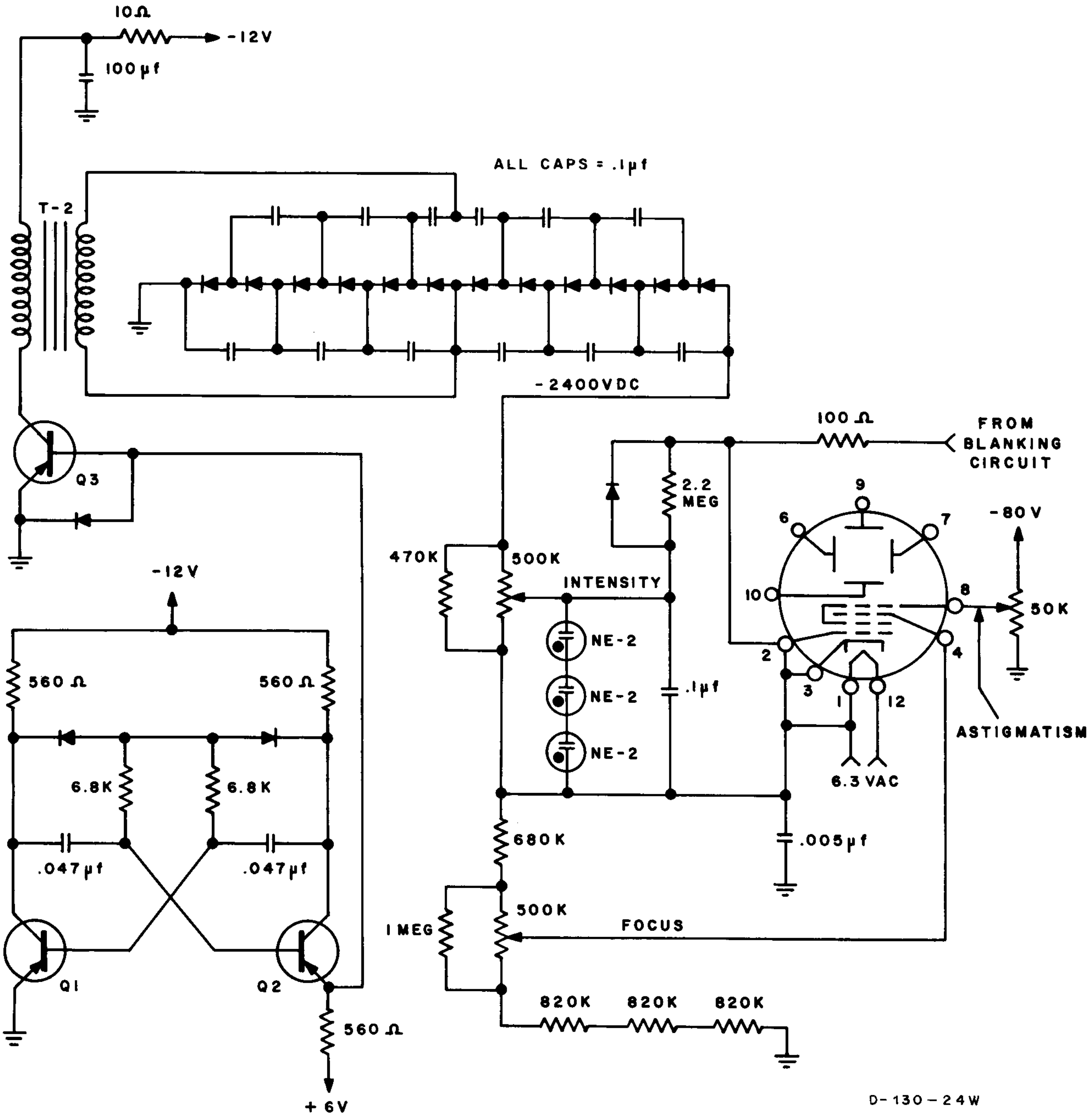


Figure 2-63. -2400 Volt Supply Schematic

M. KEYBOARD FUNCTION

1. GENERAL DESCRIPTION

The keyboard is made up of digit keys, function keys, reed switches, code bars with attached magnets that operate the reed switches, an electrical interlock, and certain mechanical interlocks.

There are eleven keys that control the entering of digits into the machine. They are the digit keys "0" through "9" and the decimal point key. There are twelve keys specified as function keys. The arithmetic functions are: Add (+), Subtract (-), Multiply (X), and Divide (÷). The data handling functions are: Change sign, Repeat, Enter, Store, and Recall. Clear Entry, Clear all, and Overflow Lock functions initiate actions to clear registers and release keyboard lockups.

2. CODE BARS

There are seven code bars with permanent magnets attached. Each code bar has cam surfaces that the key stems contact to operate the code bar into the operate or retract position. Five code bars are designated as digit code bars and two are designated as function code bars. The digit code bars are numbered "1" through "5" and are not interchangeable. The digit code bars are not spring loaded and have two positions, operate and retract. When a digit key is depressed, a beveled extension of the keystem cams all five code bars in a lateral direction. Some are cammed into the operate position and some are cammed into the retract position. Common Digit, the sixth code bar, is always operated during the selection of a digit.

Attached to each code bar is a specially shaped permanent magnet that encloses a reed switch within a hollowed portion of the magnet in an area of maximum flux lines. When the keystem cams the code bar into the operate position, the reed switch closes. If the code bar is cammed into the retract position the switch opens. The operation of the reed switches sends electrical signals to the machine for entry of the digits selected.

Once any digit code bar has been cammed to close a reed switch, the code bar remains in that position and keeps the reed switch closed until another key is depressed that retracts the code bar to open the reed switch.

The two function code bars are designated as Common Function, (CF), and Common Digit, (CD), code bars. Each has a specially shaped permanent magnet that encloses a reed switch and that closes the associated reed switch when the code bars are cammed into the operate position.

The Common Digit code bar is common to the action of all digit keys. It is spring loaded to return to its retract position upon release of any of the digit keys. Upon depression of a digit key "0" through "9", the extension on the digit key cams the Common Digit code bar in addition to setting the five digit code bars into the selected code which closes the associated reed switches. The reed switches for the digit code bars and the Com-

Depression of the digit keys causes the following code bars to operate:

DEPRESS KEY	OPERATES CODE BARS	RESTORES CODE BARS
0	none	1 - 2 - 3 - 4 - 5
1	1	2 - 3 - 4 - 5
2	1 - 2	3 - 4 - 5
3	1 - 2 - 3	4 - 5
4	1 - 2 - 3 - 4	5
5	1 - 2 - 3 - 4 - 5	none
6	2 - 3 - 4 - 5	1
7	3 - 4 - 5	1 - 2
8	4 - 5	1 - 2 - 3
9	5	1 - 2 - 3 - 4

Depression of the function keys causes the following code bars to operate:

DEPRESS KEY	OPERATES CODE BARS	RESTORES CODE BARS
Enter	3 - 5	1 - 2 - 4
Repeat	2 - 4	1 - 3 - 5
Mult	3	1 - 2 - 4 - 5
Store	2 - 5	1 - 3 - 4
Divide	1 - 3	2 - 4 - 5
Subtract	3 - 4	1 - 2 - 5
Add	4	1 - 2 - 3 - 5
Recall	2 - 3	1 - 4 - 5
Change Sign	1 - 5	2 - 3 - 4
Decimal Point	2	1 - 3 - 4 - 5

mon Digit code bars close in sequence. The reed switch operated by the digit code bars must close prior to the closure of the Common Digit reed switch. Release of the digit key permits the Common Digit code bar to return to the retract position, but the digit code bars remain in the last code position.

The Common Function code bar is common to the action of all function keys with the exception of Clear Entry, Clear All, and Overflow Lock. The depression of any of the function keys causes the beveled extension on these keys to cam the Common Function code bar in a lateral direction into the operate position, which closes the Common Function reed switch.

Attached to each function key is an adjustable magnet that closes an associated reed switch as the function key is depressed. The magnet is adjustable so that the function reed switch closes before the Common Function reed switch, and opens after the Common Function reed switch opens. Clear All, Clear Entry and Overflow Lock each have a fixed permanent magnet attached to the keystem since these are non-sequencing keys.

Release of the function key allows the Common Function code bar to return to the retract position but only after the function has been completed, because it is held in the depressed position by the function interlock.

3. KEYBOARD INTERLOCK

There are two types of interlocks in the keyboard; they are the mechanical interlock and electrical interlock.

a. MECHANICAL INTERLOCK. The mechanical interlock is a part of the code bars that the beveled extension of the keystems contact to prevent more than one key from being depressed at the same time. The Clear All, Clear Entry and Overflow Lock keys are not interlocked and can be depressed at any time.

Mechanical interlock of the digit keys is possible because each code is different and therefore only one key can be depressed at one time. Mechanical interlock of the function keys is possible because of the design of the CF code bar. When a function is selected the digit keys are blocked by the "illegal code" set up by the function key.

b. ELECTRICAL INTERLOCK. The electrical interlock consists of an electro-magnet and an armature. When a function key is depressed, the Common Function code bar is cammed into the operate position and closes the Common Function reed switch. The closure of the Common Function reed switch and associated electrical circuitry energizes the electro-magnet, and attracts the armature to the core. When the armature is attracted to the core of the electro magnet, the knife edge portion of the armature is positioned into a notch in the Common Digit and Common Function code bars. The armature is held attracted to the core until the function is completed. The function key is held depressed by a lip on the code bar that protrudes through a hole on the beveled extension of the function key. Since the Common Function code bar can not restore due to being held in the operate position, the key is held down.

4. REED SWITCHES

There are two types of reed switches used in the electronic calculator. They are: (1) Function Key switches, identified with a red dot. The leads are at a right angle to the plane of the contacts. (2) Code Bar switches, identified with a green dot. The leads are parallel to the plane of the contacts.

The twelve Function Key reed switches are operated by permanent magnets on the function keystems. The magnets are adjustable by an eccentric on all function keys except Clear All, Clear Entry, and Overflow Lock.

The seven Code Bar reed switches are operated by the magnet on the five digit code bars and by the Common Function and Common Digit code bars. (See Figure 2-64.)

The code bar reed switches operate in two modes. All of the code bars except the number "4" code bar operate in mid-mode. The number "4" code bar operates in the end mode. Due to the close proximity of other magnets, it is necessary to turn the reed switch in the opposite direction further away from other code bar magnets. All the code bar reed switches are identical; it is the manner in which they are used that makes them operate in the mid-mode or the end mode.

The reed switches are magnetically operated miniature switches that are made of thin, carefully positioned metal reeds inside a glass envelope filled with an inert gas under slight pressure. The characteristics of these reed switches are such that if a code bar magnet is positioned over the switch and moved along the length of the switch, there are three positions where the switch contacts will close and two positions where the switch contacts will open.

If the reed switch is positioned improperly with respect to the magnets in the overtravel area of the magnets, the reed switch will remain closed.

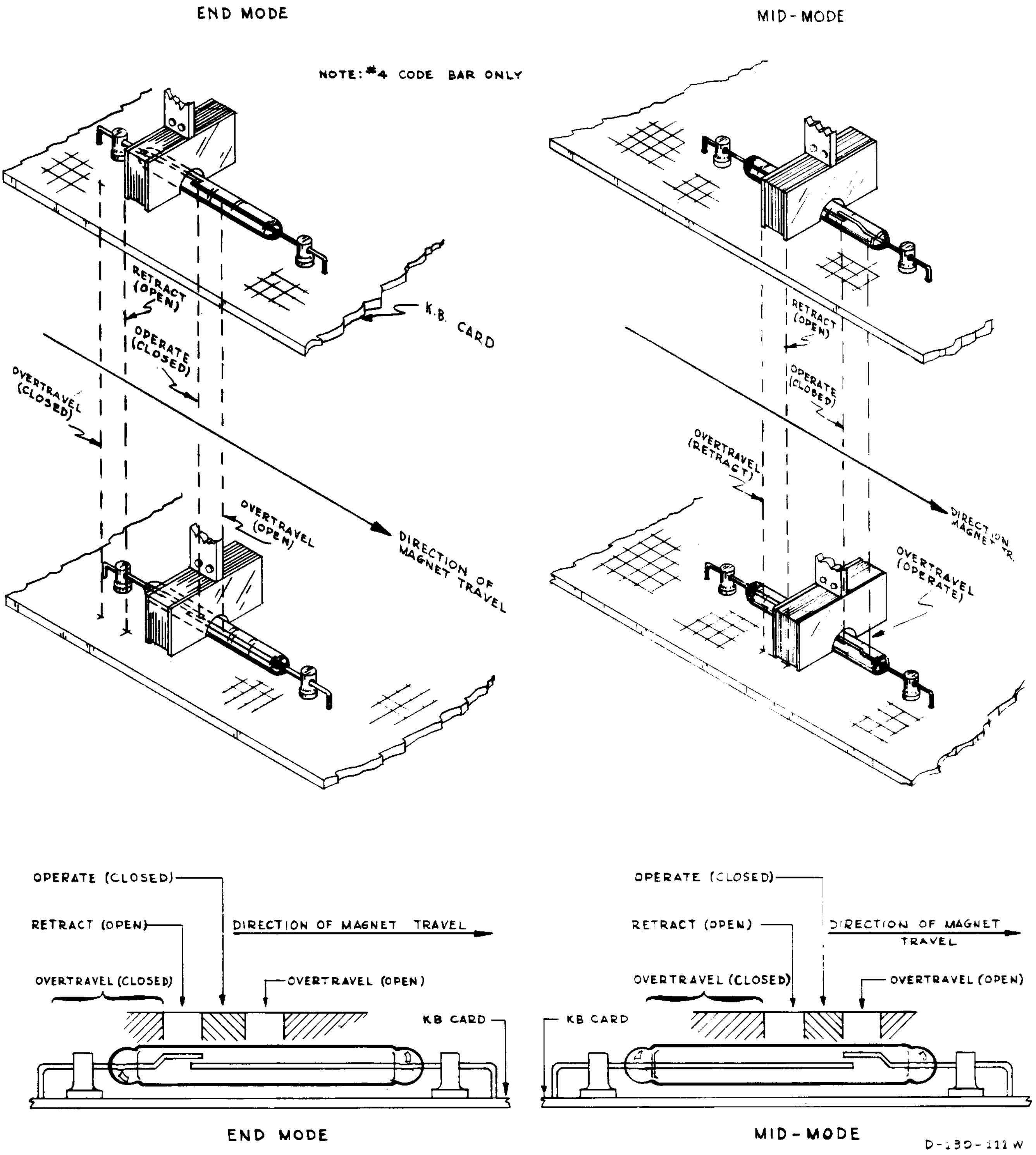


Figure 2-64. Magnet-Reed Switch Action

The travel of the magnet along the reed switch is determined by the bevel of the code bar; however, the travel is 1/2 the width of the magnet.

5. KEYBOARD ELECTRICAL FUNCTION

The purpose of the keyboard is to cause a specific machine function to occur. Typical functions are Digit Entry, +, -, X,(÷), etc. This section discusses the way the keyboard electrical circuits are acted upon by the machine logic and vice-versa.

a. KEYBOARD INTERFACE. The keyboard interface cards, (J and K), make up the circuitry between the keyboard and the internal logic components. These cards contain the reed switch filters which are used to help reduce the electrical effects of contact bounce inherent in the reed switches.

Also mounted on the J card are two transistors that are a part of the interlock coil circuit, and four diodes that form the input OR gate of the Keyboard Pulse Generator, (KBD), circuit.

(The J and K boards are being replaced by a single card that will be called the JB card. The electrical action is the same, whether on the J and K cards, or on the JB card.)

b. KEYBOARD DELAY CIRCUIT: With the exception of the input OR gate which is located on the J card, the KBD circuit is physically located on the B card. Electrically it connects the reed switch filters and the machine logic elements. As the name implies, this circuit delays the effect of the closing of the reed switches, and in so doing eliminates any remaining contact bounce. The four reed switches that initiate a keyboard delay signal are: Decimal Point, Clear Entry, Common Function, and Common Digit. The output of the delay circuit is EKBD3, and the transition from False to True is the useful output. (See Figure 2-65.)

With the four reed switches open, Q1 is biased on by the voltage divider in its base circuit. Now, when any one of the inputs goes True, (0 volts), Q1 turns off. Just prior to Q1 being turned off, its collector is at ground, and C1 has no charge. When Q1 turns off, C1 must begin to charge toward -80 volts. In about 6 milliseconds the upper plate of C1 reaches -12 volts. Now, when the emitter of Q2 goes slightly more negative than its base, which is returned to -12 volts, Q2 turns on. Thus, there is a delay of about 6 milliseconds between the time Q1 turns off and Q2 comes on. (The actual delay is subject to wide variation due to component tolerance, and the circuit will work if the delay is greater than about 3 milliseconds.)

When Q2 begins to turn on, it turns on Q3, which helps Q2 to go further on, which drives Q3 on harder. Q2 and Q3 are connected in a "regenerative loop" and the reason for this is simply to generate a fast risetime on the output pulse. The output pulse goes from -12 volts to -1.5 volts as Q3 turns on. The regenerative action of Q2 and Q3 insures a risetime of at least .2 microseconds, which is necessary, or at least desirable, to properly operate the logic circuits.

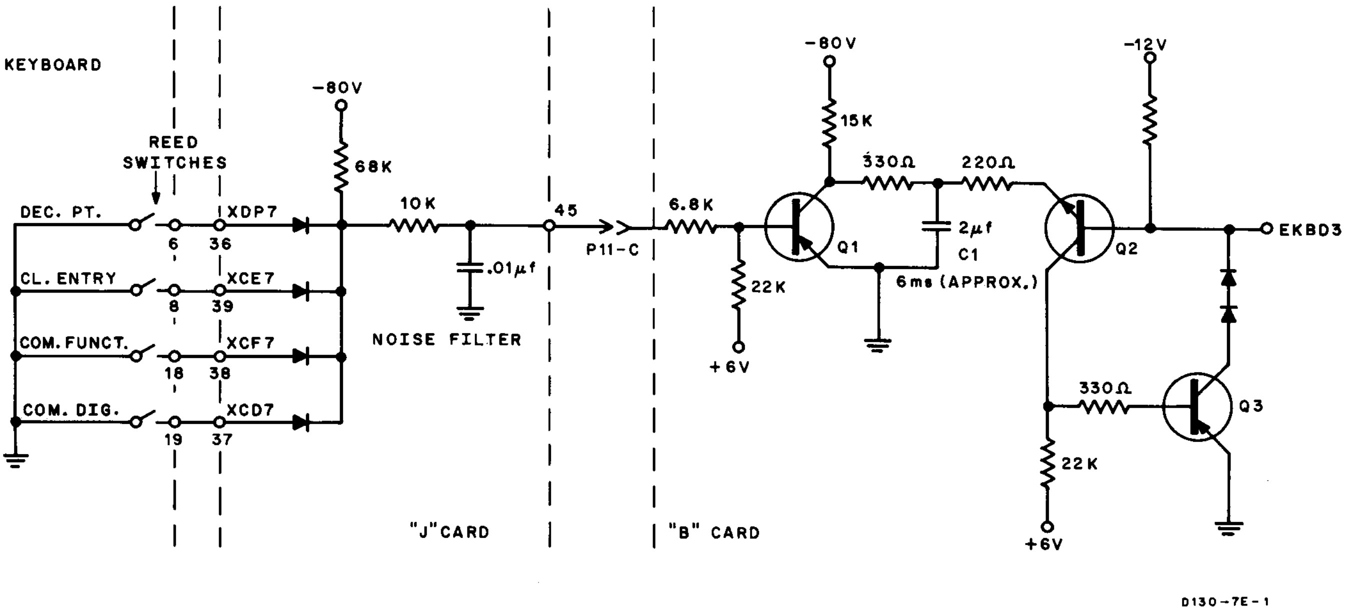


Figure 2-65. Keyboard Delay (KBD) Schematic

The RC combination, (10K and .01 µf) connected between the OR gate and Q1, acts as a noise filter to help remove noise from the signal.

c. KEYBOARD LOCKUP. The keyboard is locked up during a function and during register overflow conditions that may occur in the machine logic.

(1) Function Lockup. The Common Function, (CF), code bar is locked in operate position during a function until the function is complete. This is accomplished by energizing the lockup electro-magnet which places a latch into a recess on the CF code bar and prevents the code bar return spring from bringing the code bar to retract position.

Energizing the lockup magnet during a function is controlled by ECF1 at an OR gate (Figure 2-66). When CF FF sets at the beginning of a function, ECF1 goes True at this OR gate. The True output of the OR gate is inverted False (-12 volts) and applied to heavily turn on an inverter connected in series with ground, the interlock solenoid coil, and -12 volts. When this inverter turns on, effective ground appears at the magnet coil and current flows through the coil from -12 volts, which energizes the coil keeping the CF code bar locked in operate position. When the CF FF resets at the end of the function, ECF1 goes False and the lockup magnet releases, which permits the CF code bar return spring to bring the CF code bar to retract position.

During the time CF code bar is held in operate position, the particular function key chosen sets an illegal mechanical notch-code into the digit code bars, which prevents the digit keys from being depressed. The other function keys cannot be depressed because CF code bar is held fixed. The keyboard is thus locked up during a function and is not released until CF FF resets at the end of the function.

(2) Number Entry Overflow. The EC-130 entry register can contain 13 digits. If more than 13 digits are entered an overflow condition exists and the keyboard locks up. (See Figure 2-66.)

Number Entry lockup is controlled by O-066. ME1L3 will be True at this gate during the entering of each digit until the shift left of previously entered digits is completed. ME1L3 True through O-066 is inverted False by I-067, designated M1L4, and M1L4 False enables O-106. During a Number Entry, MMDL3 which specifies Multiply or Divide function will be False. (HOME1 has no logic function but improves RSL05 pulse shape.)

Now, when TC154 goes False, denoting C15 time, the output of O-106 goes False. O-106 False is inverted True by I-107, designated R1OF3 (Register 1 Overflow). R1OF3 True is applied through O-300 as RSL05 to an AC gate on set input of Overflow FF. If CDZ4 is True at this AC gate, which would indicate significant data in D Counter, Overflow FF sets.

CDZ4 True at C15 time means that significant data has been placed in D Counter by the C14 shift left. Since C14 is the last of the display columns, there is no further column in which to place this D Counter data, thus an Overflow condition. In other words, machine capacity has been exceeded.

(3) Decimal Align Overflow. When any function key is pressed, the number in R1 shifts left until the whole number portion is to the left of the chosen decimal position. Assume the decimal position is on 5. This indicates that there are 8 possible columns for whole number digits to the left of the decimal point. Now, if a number with 9 whole number digits is decimal aligned, an overflow condition will exist. This overflow condition is indicated by the lighting of OVERFLOW LOCK Key, and Keyboard Lockup. This is controlled by the same gates as during Number Entry when entering too many digits (more than 13). The only difference is the initiating logic signal on O-066, which in the case of Decimal Align is MA1L3. MA1L3 will be True until all shifts left are completed and is applied to O-024 at the Entry Phase Counter which keeps HOME from stepping EPC, and also to O-029. MA1L3 True at O-066 enables Overflow FF set through the logic, but at O-029 MA1L3 True inhibits AOFL3 True until all the shifts left are complete. Then, MA1L3 goes False and AOFL3 then goes True which is applied to gate 1103 on CF-FF. MAIL3 False will now allow HOME to step the EPC via O-024. Simultaneously when HOME does step EPC to 2, it resets CF-FF via Gate 1103. ECF1 on O-16 generates ECFD4 True from I-017 which clamps the EPC to 0. The keyboard remains locked up because of AOFL3 to the interlock coil. The misentered number is displayed in R1 and the Overflow light is ON.

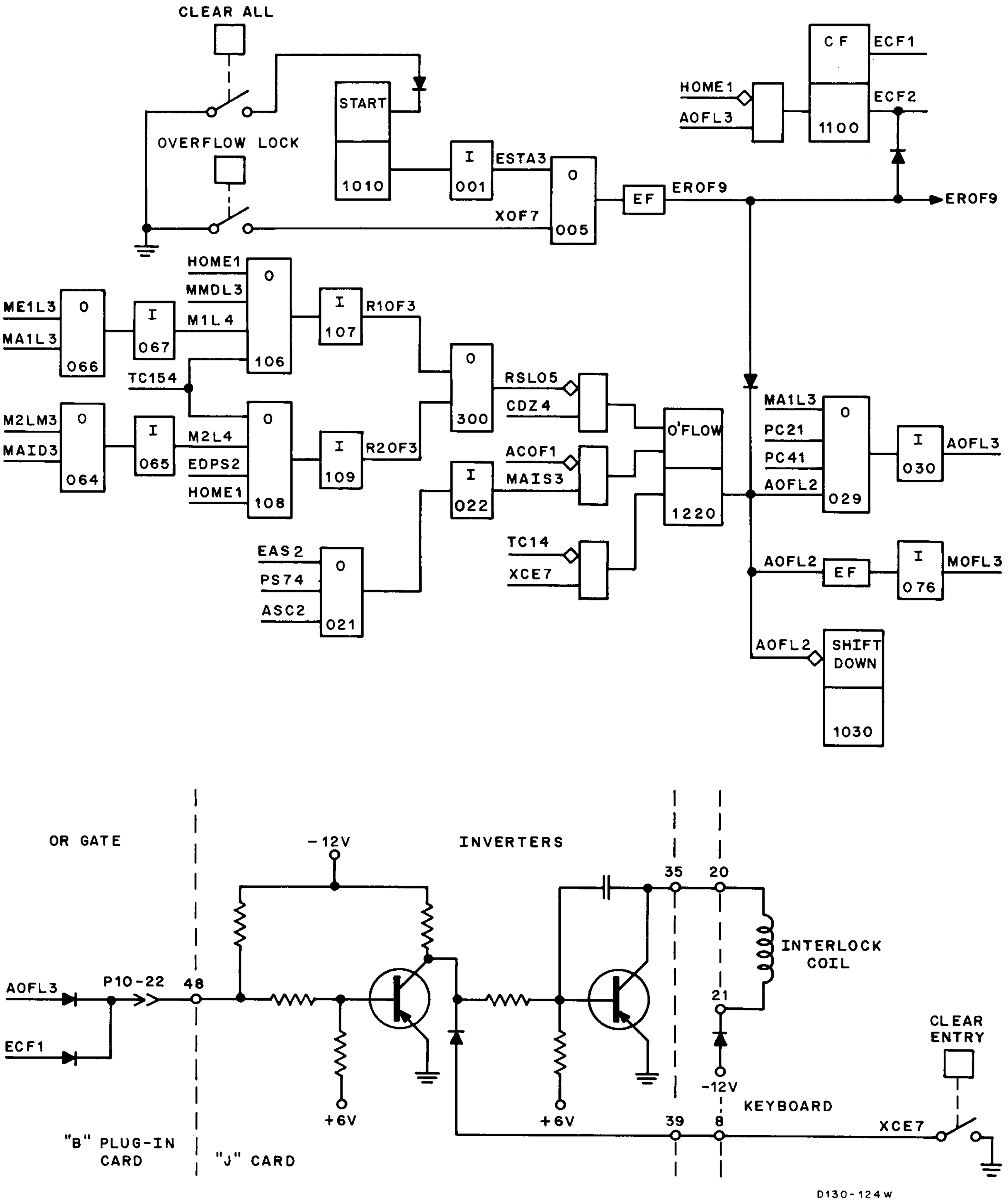


Figure 2-66. Overflow Logic and Interlock Coil Schematic

(4) Multiply or Divide Overflow. During the progress of arithmetic operations an overflow condition may be created. The specific conditions will be discussad under Function conditions will be discussed under Function Logic as applicable. As specifically related to the Overflow lock-up solenoid circuit however, the action in Multiply or Divide is that at gate O-064, either M2LM3 will be True in Multiply, or MA1D3 True in a Divide. True output of O-064 is inverted False by I-065, designated M2L4 (Shift R2 left). M2L4 enables O-108. If DPS is set, denoting that the answer is being decimal aligned in R2, DPS2 is False at O-108. When TC154 goes False, O-108 output is False. (HOME1 has no logic function but improves the pulse shape of RSL05).

False output of O-108 is inverted True by I-109, designated R2OF3 (R2 overflow). R2OF3 True is applied through O-300 (RSL05) as an AC transition to an AC gate on Overflow FF. At this time, if there is data in D Counter, which would indicate part of the answer is in D and no further display column available, CDZ4 will be True, and Overflow FF sets. The setting of Overflow does not cause the machine to step to zero as in decimal align because AOFL3 cannot be generated after EPC step 1. This logic control allows the machine to complete the problem by decimally aligning the answer. Because of this a 26 digit product can be realized, i.e., the lower digits of an answer whose product exceeds register capacity.

(5) Add Function Overflow. At O-021, EAS2 will be False during Add or Subtract; PS74 will be False during EPC7; and ASC2 will be False during Add function. False output of O-021 is inverted True by I-042, designated MAIS3. MAIS3 True enables an AC gate at set input of Overflow FF. Now, when ACOF1 goes True, Overflow FF sets. ACOF1 will go True if Carry is set at Home time during an Add function. Carry being set indicates a carry of one to the next column, and Home time signifies no more columns. Since the Carry is a valid part of the addition, as overflow condition exists which is signified by set of Overflow FF as described in Number Entry overflow.

d. KEYBOARD LOCKUP RELEASE. Keyboard lockup is cleared by depressing OVERFLOW LOCK key, CLEAR ENTRY key, or CLEAR ALL key.

(1) Overflow Lock Release. OVERFLOW LOCK key makes XOF7 True by reed switch action. XOF7 True at O-005 makes O-005 output True. O-005 True output is applied through an emitter-follower as EROF9 to reset, in particular, CF and Overflow FF's. Reset of Overflow FF makes AOFL3 False, which opens the interlock coil circuit and releases the solenoid latch. At the same time, CF reset makes ECFD4 (I-017) True, which clamps EPC to 0, and enables Display.

(2) Clear Entry Lockup Release. CLEAR ENTRY key makes XCE7 True by reed switch action. XCE7 True is applied through an isolation diode to the inverter controlling interlock coil current, and turns off the inverter. When the inverter is off, the solenoid current is interrupted and lockup is released. At the same time, XCE7 True enables an AC gate on Overflow FF reset input. Now, when TC154 goes True, Overflow FF resets. When Overflow resets, AOFL2 goes True and sets Shift Down FF, which in turn enables R1 through R4 to shift down one register. This shift down places R1 data, which caused the overflow, into R0 where it is replaced by the initiation of any arithmetic function, thus is effectively discarded. (See Clear Entry discussion under Function Logic). This is a special means of setting Shift Down FF because the usual method which utilizes EKBD3 is blocked by the keyboard lockup condition.

(3) Clear All Lockup Release. CLEAR ALL key makes XCA7 True through reed switch action. XCA7 True is applied through an isolation diode to set output of Start FF, and Start FF sets, which makes ESTA2 False. ESTA2 False is inverted True by I-001, designated ESTA3. ESTA3 True at O-005 makes EROF9 True. EROF9 is applied to reset, in particular, CF and Overflow FF's. Reset of Overflow removes lockup, and reset of CF makes ECFD4 True, which clamps EPC to 0. Meanwhile, ESTA3 True at an OR gate in the Write Amplifier inhibits writing data on the line, which removes all data from the machine. (See Clear All Function Logic.)

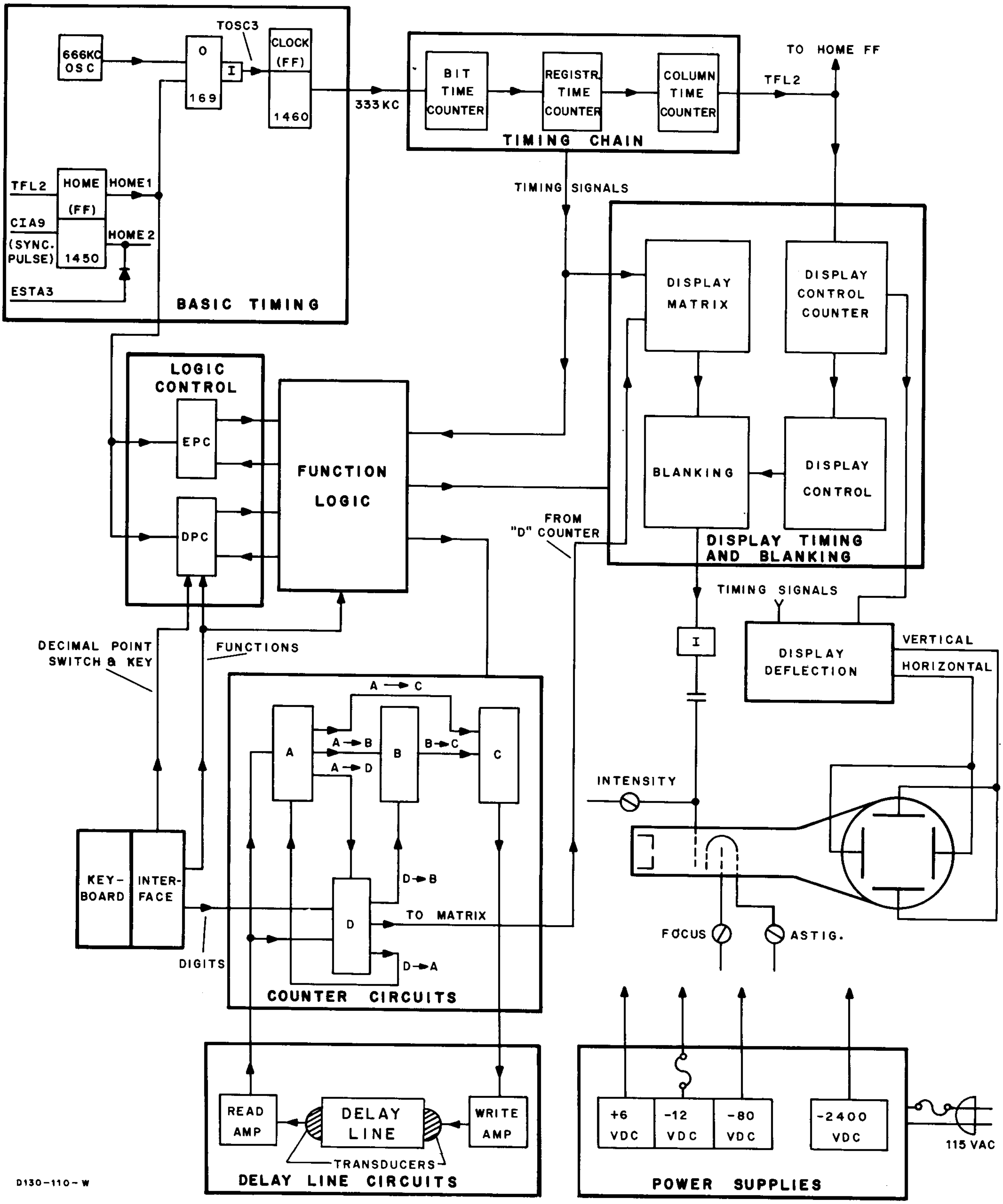


Figure 2-1. Overall Block Diagram

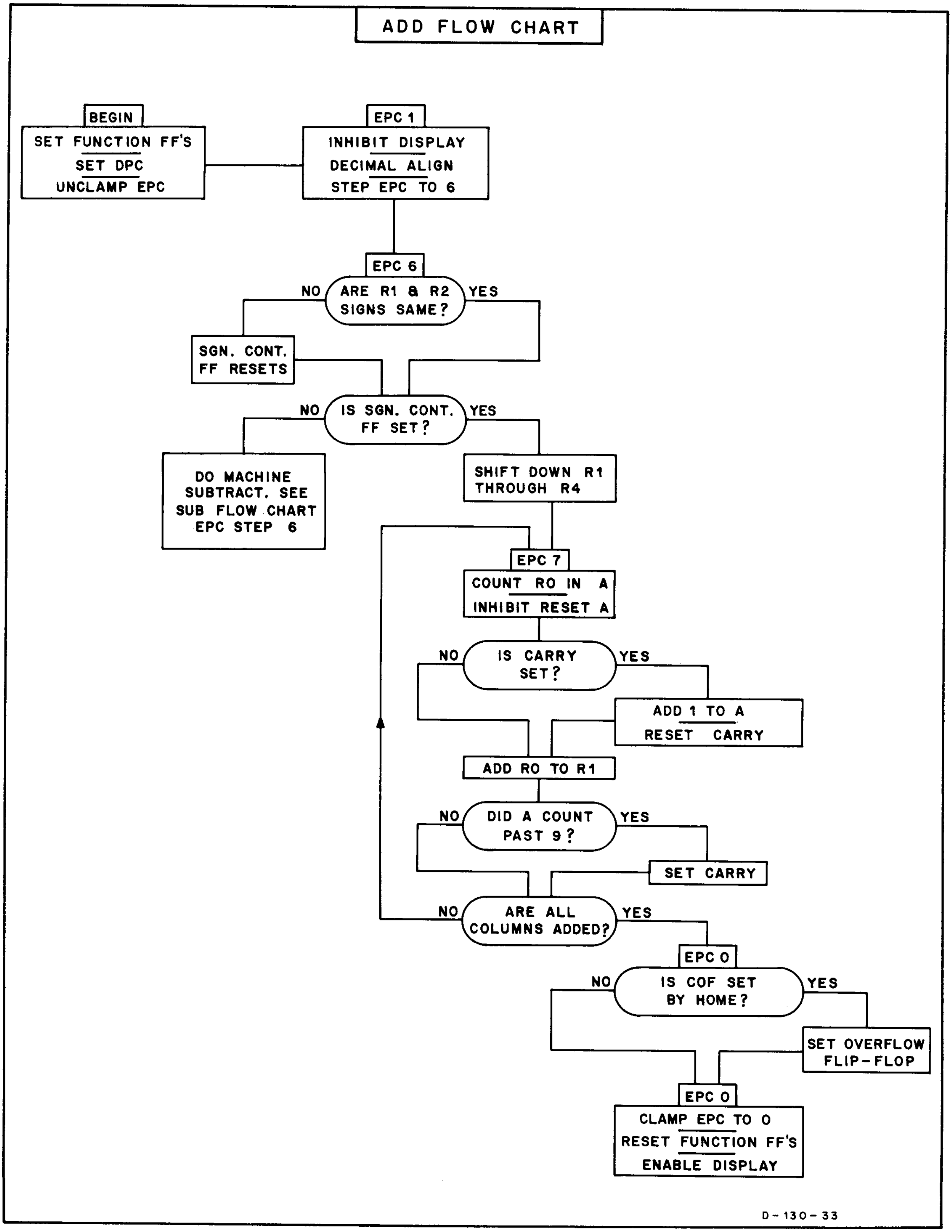


Figure 2-29. Add Flow Chart

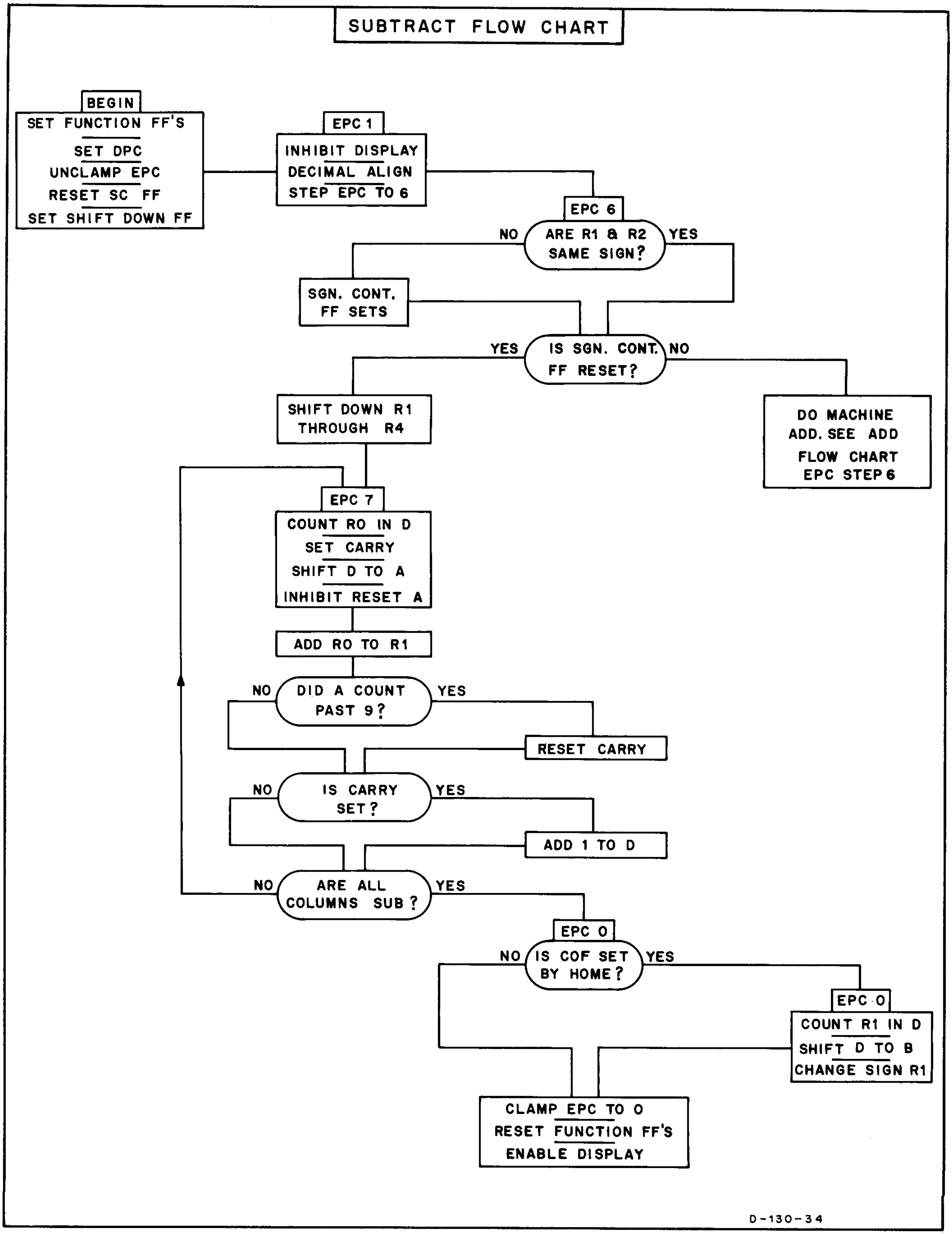


Figure 2-30. Subtract Flow Chart

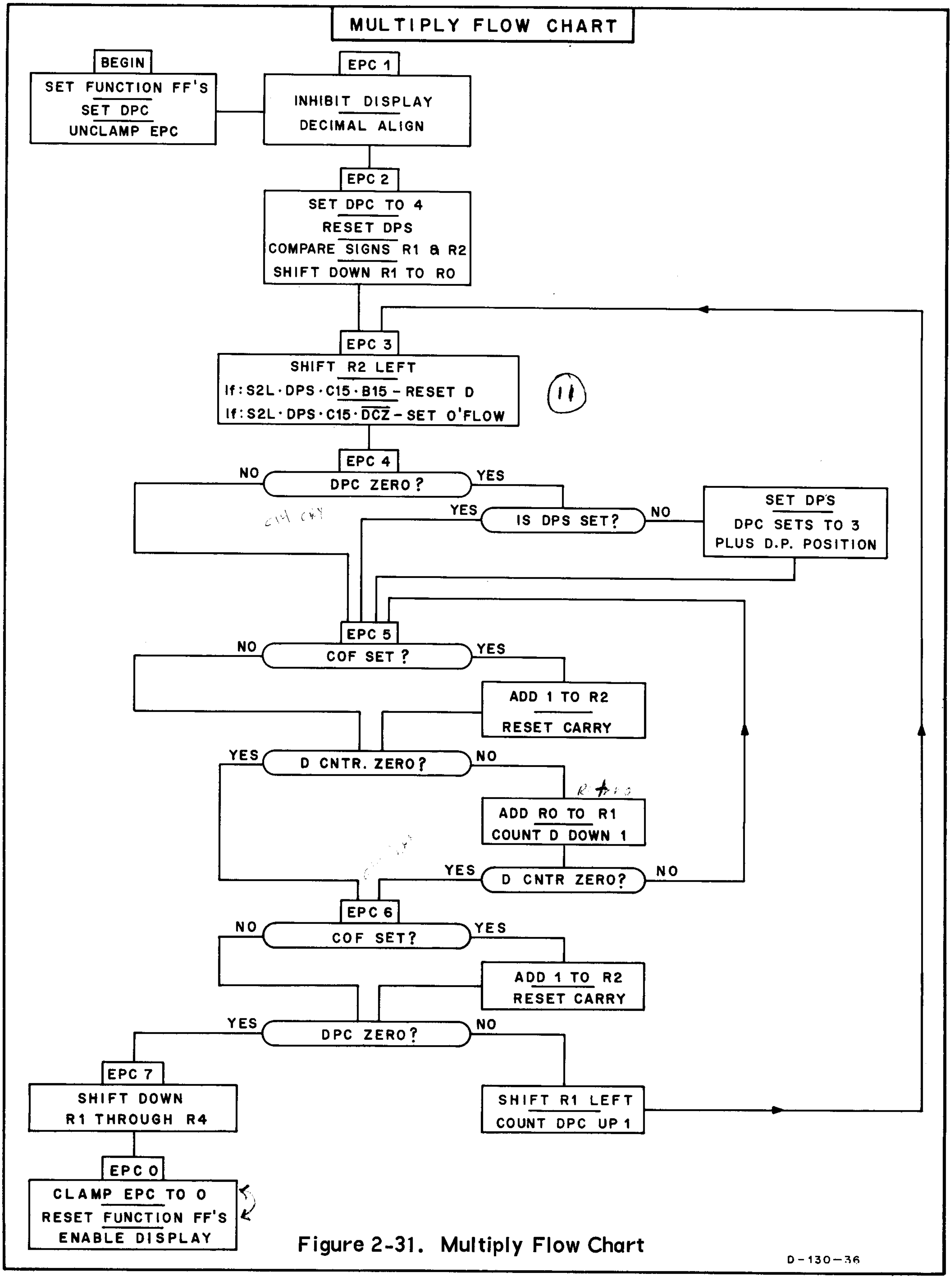


Figure 2-31. Multiply Flow Chart

D-130-36

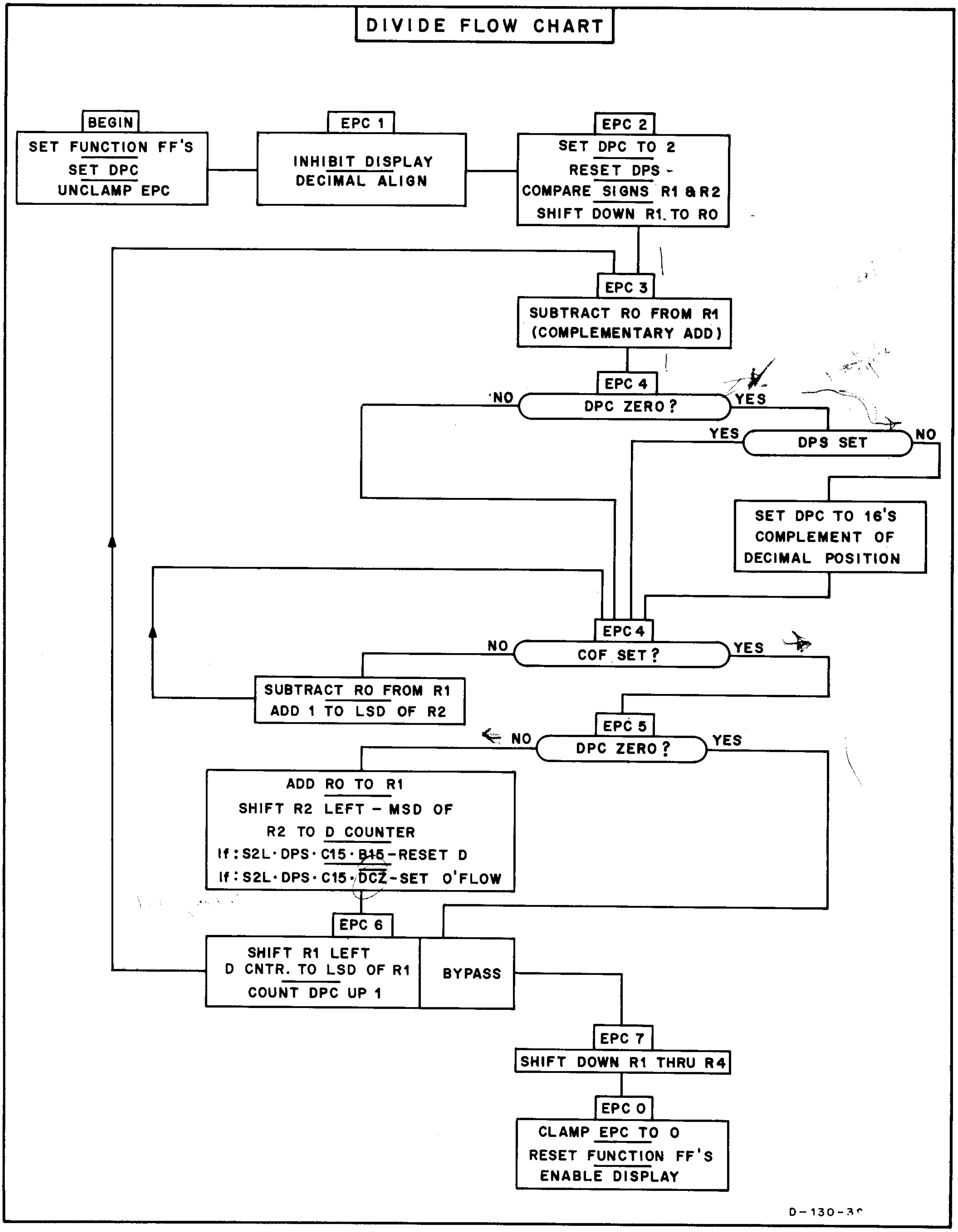


Figure 2-32. Divide Flow Chart

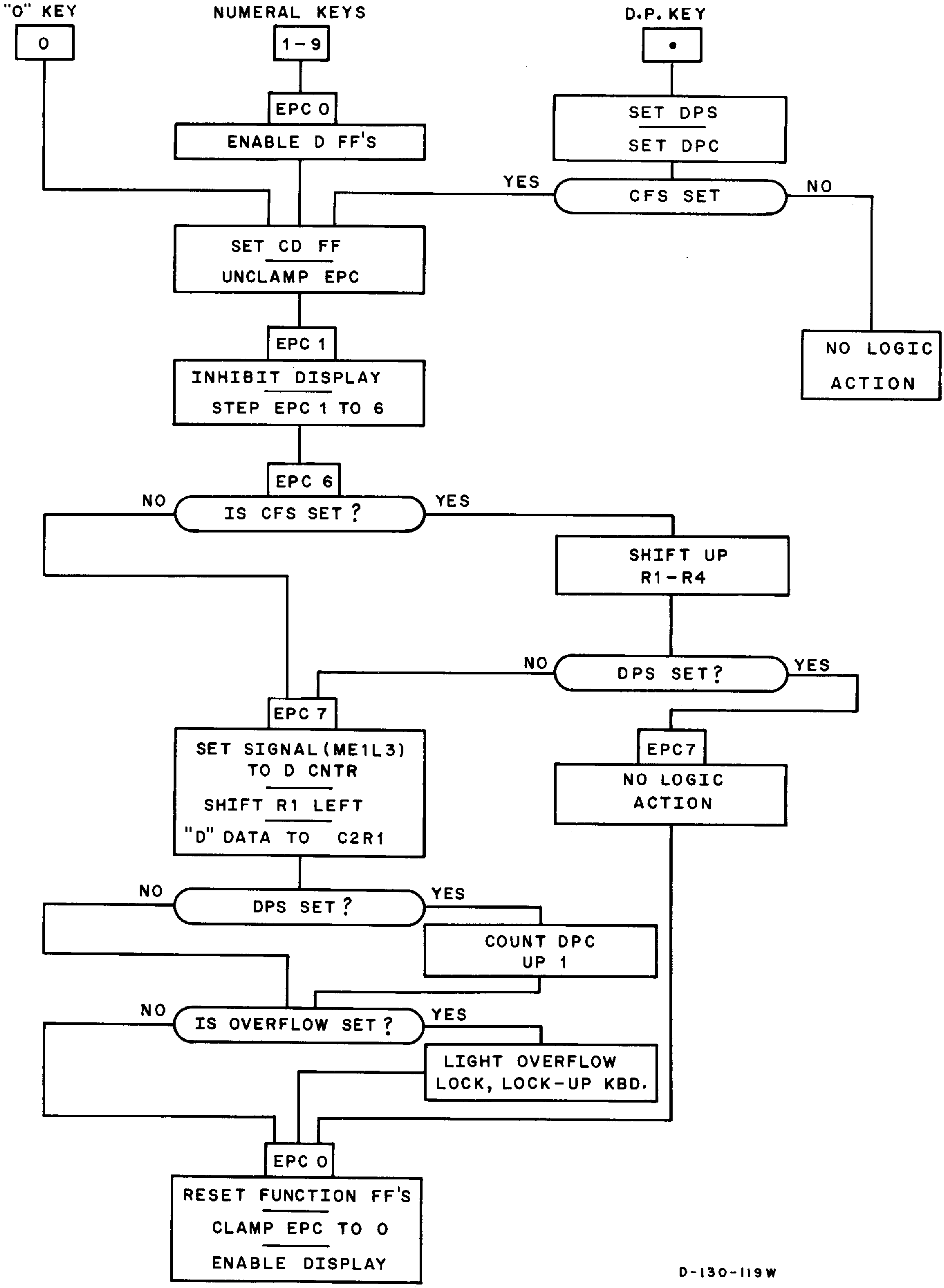
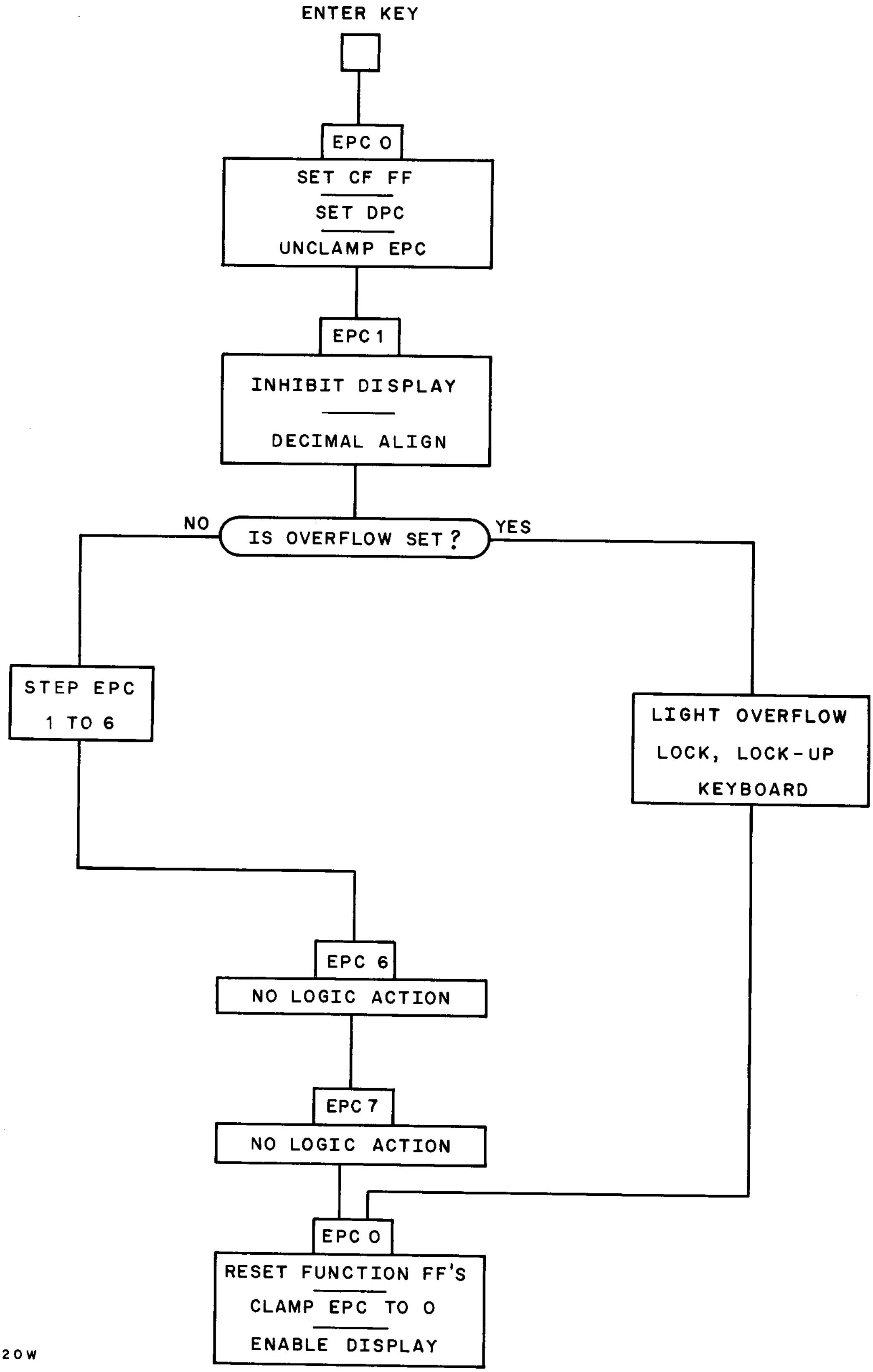


Figure 2-34. Digit Selection Flow Chart



D130-120W

Figure 2-35. Enter Flow Chart

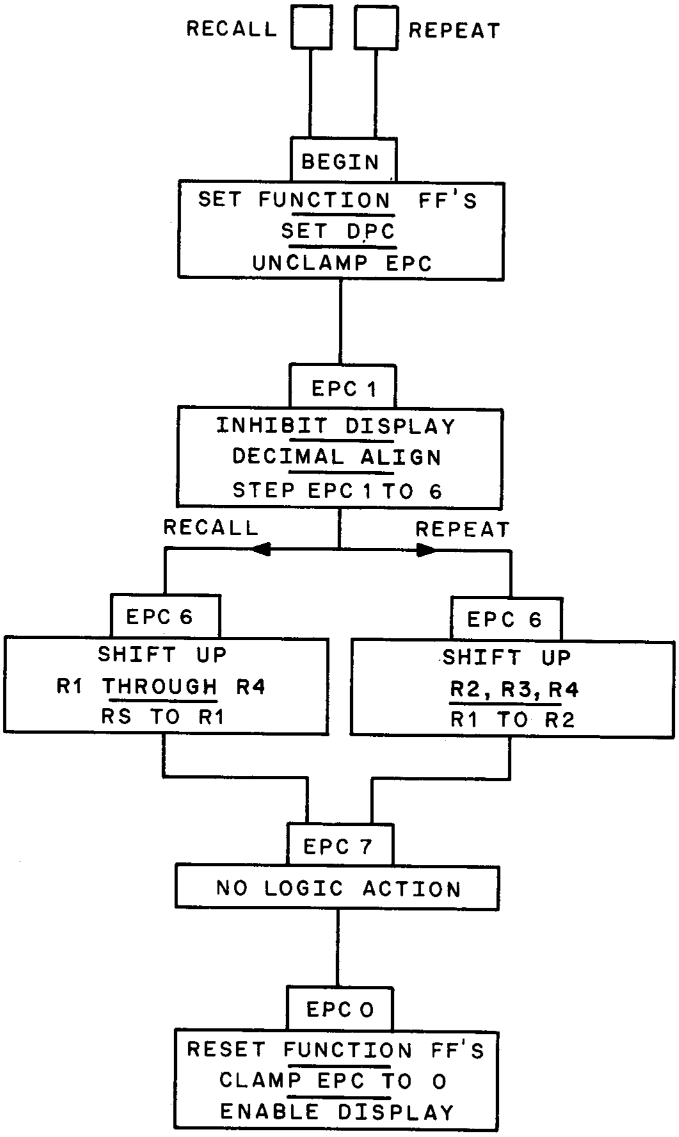


Figure 2-37. Repeat and Recall Flow Chart

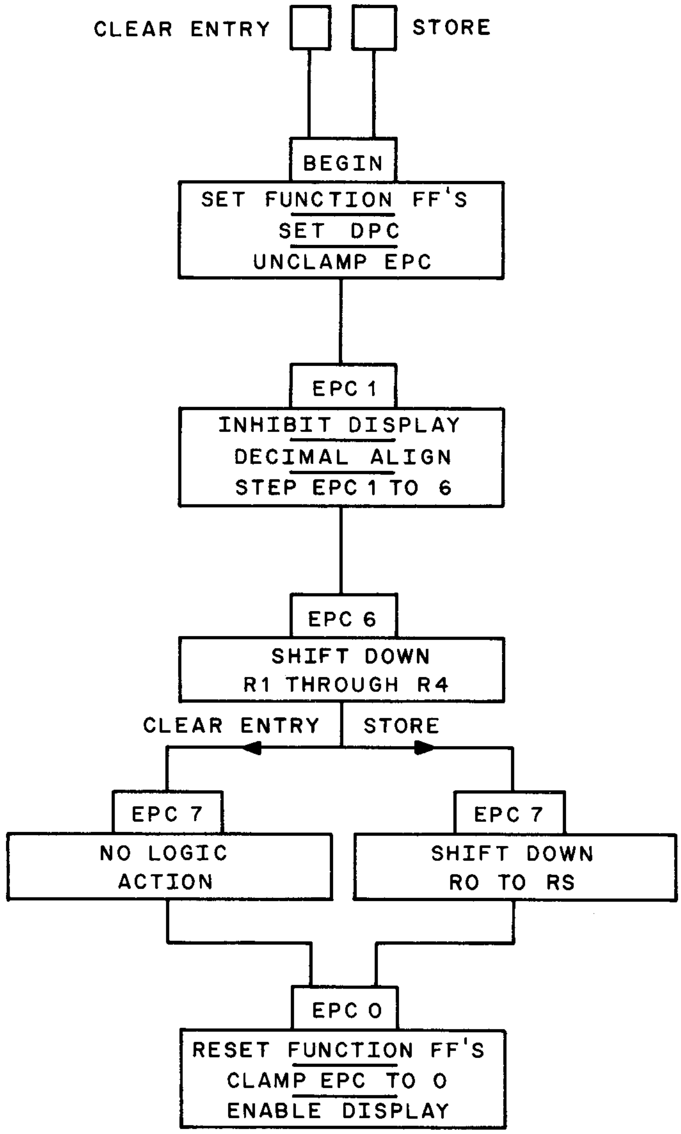


Figure 2-39. Clear Entry and Store Flow Chart

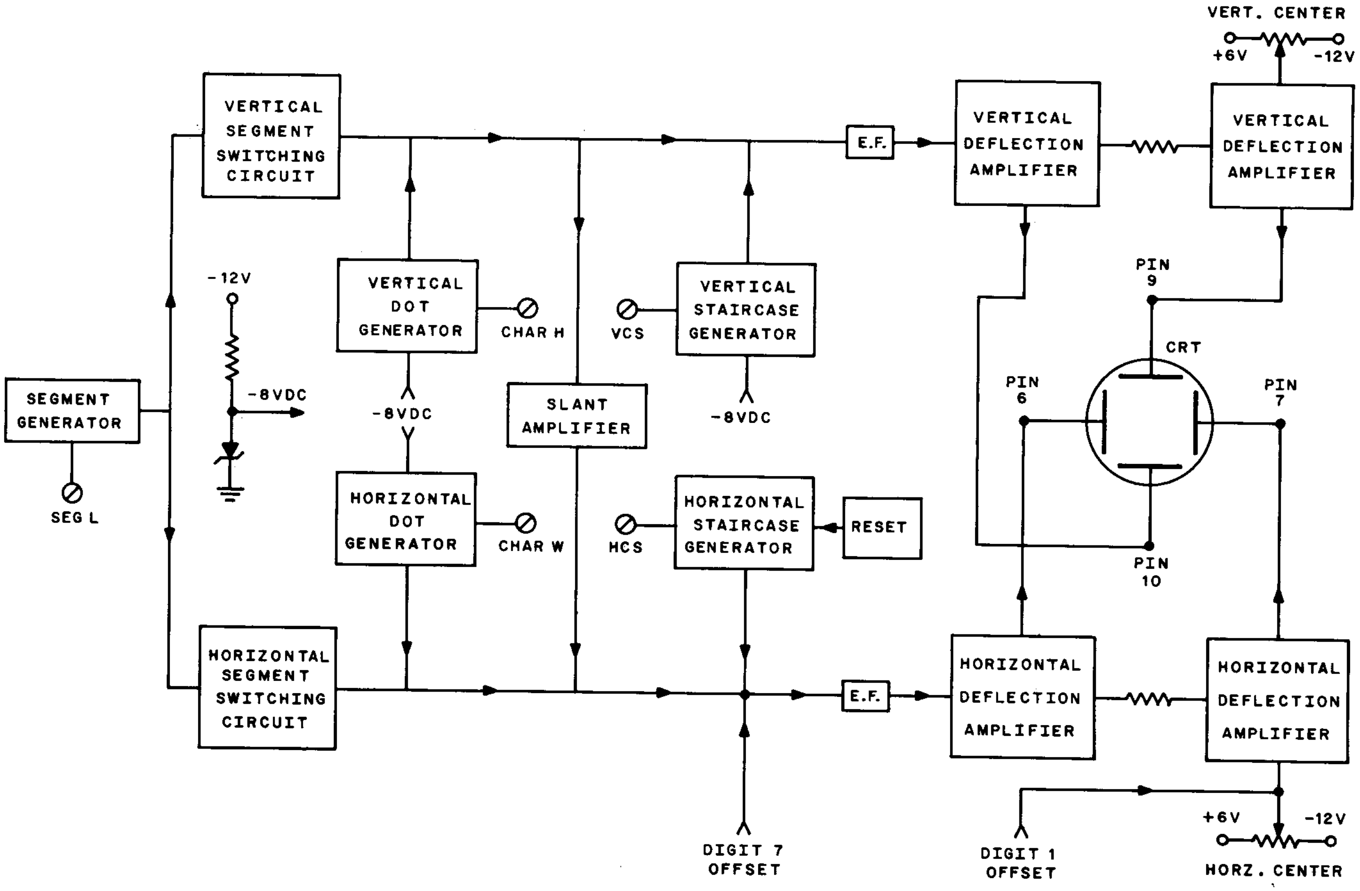

VERT. CENTER
+6V
-12V
VERTICAL SEGMENT SWITCHING CIRCUIT
E.F.
VERTICAL DEFLECTION AMPLIFIER
VERTICAL DEFLECTION AMPLIFIER
-12V
VERTICAL DOT GENERATOR
CHAR H
VCS
VERTICAL STAIRCASE GENERATOR
PIN 9
CRT
SEGMENT GENERATOR
-8VDC
-8VDC
SLANT AMPLIFIER
-8VDC
PIN 6
PIN 7
SEG L
HORIZONTAL DOT GENERATOR
CHAR W
HCS
HORIZONTAL STAIRCASE GENERATOR
RESET
PIN 10
HORIZONTAL SEGMENT SWITCHING CIRCUIT
E.F.
HORIZONTAL DEFLECTION AMPLIFIER
HORIZONTAL DEFLECTION AMPLIFIER
+6V
-12V
DIGIT 7 OFFSET
DIGIT 1 OFFSET
HORZ. CENTER

Figure 2-42. Deflection Circuits, Composite Block Diagram

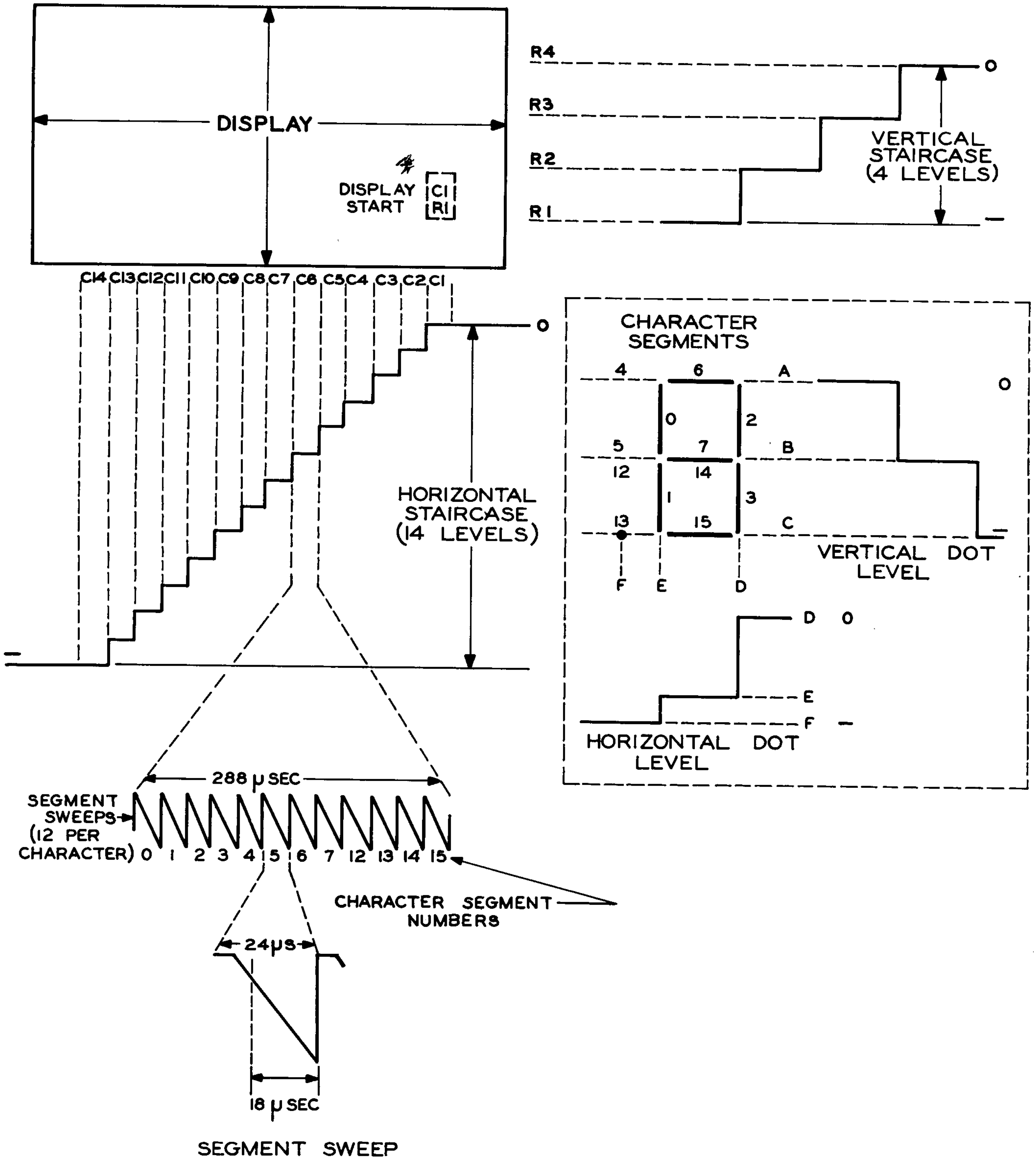


Figure 2-49. Deflection Voltage Relationships

SECTION 3 - ADJUSTMENTS

A. SCOPE OF SECTION

This section contains the adjustments necessary to ensure proper operation of the EC-130. Certain adjustments that are obvious to trained service personnel such as INTENSITY, FOCUS, etc. are not included.

B. KEYBOARD ADJUSTMENTS

The keyboard adjustments are those adjustments necessary for the proper functioning of the keys on the keyboard. These adjustments should not be made unless thorough checking has established that the machine malfunction is definitely in the keyboard.

1. EQUIPMENT REQUIRED

Special items of equipment as well as normally available tools are required to adjust the keyboard. They are as follows:

a. Keyboard Tester, or VOM Adapter (Figure 3-3).
b. Screwdriver
c. Soldering Iron
d. Long Nose Pliers
e. Plastic Probe

2. INITIAL PROCEDURE

Before proceeding with any keyboard adjustment, perform the following:

a. When using Keyboard Tester (Figure 3-1):

(1) Disconnect wires on taper pins on bottom of keyboard.

(2) Connect Keyboard Tester Cable to taper pins on keyboard, carefully observing tester cable to taper pin number coding.

(3) With long nose pliers, remove interlock solenoid taper pin connections through access hole in front of keyboard. Pull wires gently through access hole and connect alligator clip leads from Keyboard Tester.

(4) Connect Tester to AC line, and turn Tester POWER switch to ON.

(5) Press digit keys 1 through 9 in turn, and observe that associated lamp numbers (1-5) come on before Common Digit (COM DIG) light comes on (See Figure 3-2).

NOTE: Before pressing each digit key depress 0 key, which places all digit code bars to retract position.

(6) Press #5 key, then press digit keys 0 through 9 in turn, and observe that associated lamp numbers (1-5) go off before COM DIG light comes on.

NOTE: Before pressing each digit key depress 5 key which places all digit code bars to operate position. During testing of digit keys, check that COM DIG lamp comes on last during depression of a key, and goes off first during release.

(7) Press, in turn, the following sequencing function keys: Store, Recall, Repeat, Change Sign, Add, Subtract, Multiply, and Divide.

(8) When pressing a sequencing function key, observe for the following:

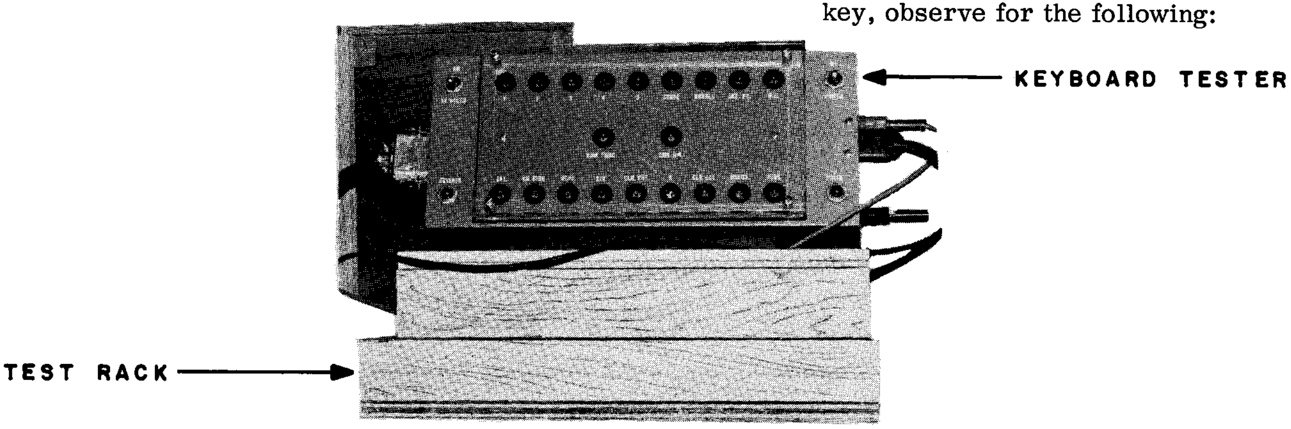


Figure 3-1. Keyboard Tester

(a) That named lamp on tester comes on first during depression, and goes off last during release.

NOTE: Each function key also lights certain digit lights. This is a mechanical interlock of the digit code bars and should be as indicated on Tester Lamp Chart (Figure 3-2).

(b) That Common Function (COM FUNC) lamp on tester comes on last during depression, and goes out first during release.

(c) That COM FUNC lamp on Tester comes on before key bottoms. This is called "over-travel", and there should be a small amount.

(9) Press, in turn, the following non-sequencing function keys: Overflow Lock, Clear Entry, Clear All, Decimal Point.

(10) When pressing a non-sequencing function key, observe that the associated lamp on the Tester comes on before bottoming of the key.

(11) Press Enter key and observe that COM FUNC lamp on Tester comes on before bottoming of the key.

b. When using VOM and Adapter:

CHECKING SEQUENCE:

The volt ohm meter is zeroed on the X10 scale and connected in series with the test circuit as shown in Figure 3-3.

(1) To check common digit in relationship to closure of digits "0" through "9": Connect black wire to the CD switch, pin 19. Connect the five (5) white wires to pins 1, 2, 3, 4, 5. Connect COM lead of meter to pin 24.

(2) Depress "0" key and release. This restores all code bars. The VOM reading should be infinity. Any other reading would indicate one (1) or more reed switch has remained closed. Disconnect each white wire and the black wire, one at a time, to determine the closed or shorted reed switch.

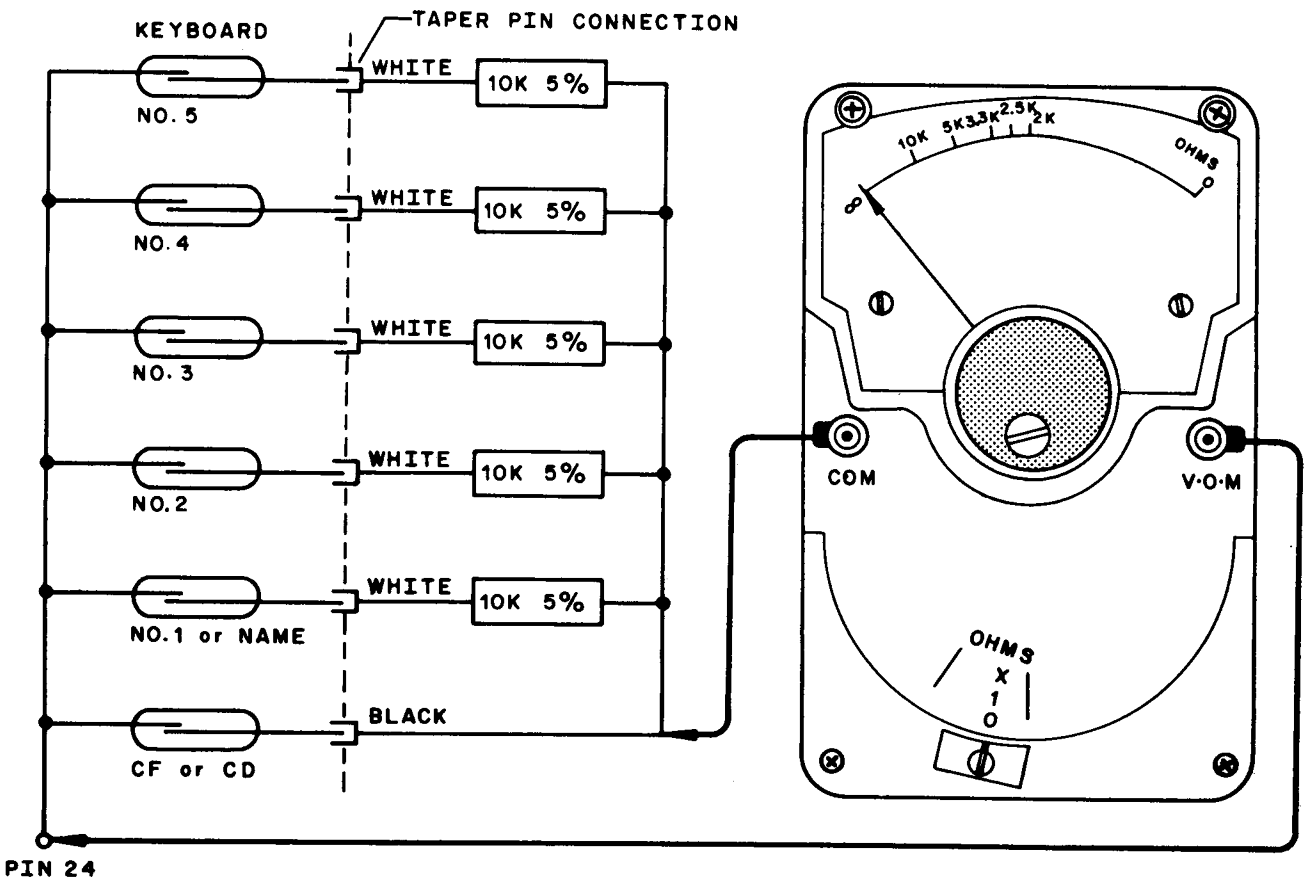


Figure 3-3. VOM Adapter Schematic

(3) Operational sequence check.

(a) Depress 0 key slowly to pad. Reading jumps from infinity to 0.

(b) Depress 1 key slowly to pad. Reading changes to 10K then jumps to 0. Release key, reading is now 10K. This is due to the fact that there are no return springs on any of the digits one (1) to five (5) code bars and the code bars remain operated thus keeping the reed switch closed.

(c) Depress 0 key slowly to pad. Reading jumps from 10K to infinity and then to 0.

(d) This procedure is to be completed with each digit key. It is necessary to understand of course that the digit 5 key will have a lower ultimate reading before going to 0. This is due to placing more resistors in parallel before the operation of CD switch.

(e) A program to follow that checks both the opening and the closing of the numbered reed switches before closure of the common digit switch is as follows: Press, check, and release each key as shown.

0 - 1 - 0 - 2 - 0 - 3 - 0 - 4 - 0 - 5 - 0 - 6 - 0 - 7 - 0 - 8 - 0 - 9 - 0.

This test will check that each code bar reed switch is operated prior to the common digit switch. The ohm meter reading must reach its ultimate value, as listed in Figure 3-4 chart, prior to the closing of common digit and will probably, but not necessarily, reach this value in incremental steps as the individual switches are opened or closed.

Another test would be to press, check, and release each key in the following manner:

5 - 0 - 5 - 1 - 5 - 2 - 5 - 3 - 5 - 4 - 5 - 6 - 5 - 7 - 5 - 8 - 5 - 9 - 5 - 0.

This will check the ability of the code bar reed switches to open prior to the operation of the common digit reed switch.

Operation of the function reed switches, in relation to the Common Function switch, may be checked by removing all white wires from the numbered reed switch and connecting one (1) of these wires to the function reed switch to be checked. This will then show a meter movement from infinity to 10K ohms and then to zero (0) ohms, as the switch is operated, and from zero (0) ohms to 10K ohms to infinity, as the switch is released.

3. CD REED SWITCH

The adjustment of a digit key is to ensure that the lamp, or lamps, on the Tester associated with that key come on before COM DIG lamp, and the COM DIG lamp comes on before key bottoming (giving overtravel). To adjust CD Reed Switch proceed as follows:

a. Determine whether CD lamp is lighting early or late.

CAUTION: Turn off Tester between soldering operations.

b. On underside of keyboard, unsolder cradle slide specified CD (See Figure 3-5).

c. Move cradle gently right or left until COM DIG lamp on Tester just comes on. (See Figure 3-2.)

d. Resolder cradle slide in new position, being very careful not to change cradle position.

e. Check that digit key has overtravel after COM DIG lamp comes on.

4. DIGIT KEY REED SWITCH

a. Determine which digit lamp is lighting early or late.

b. On underside of keyboard, unsolder cradle slide designated for the lamp (1-5) that is early, or late.

c. Gently move cradle slide to the right or left until specified lamp, or lamps, come on or go off, as applicable. (See Figure 3-2.)

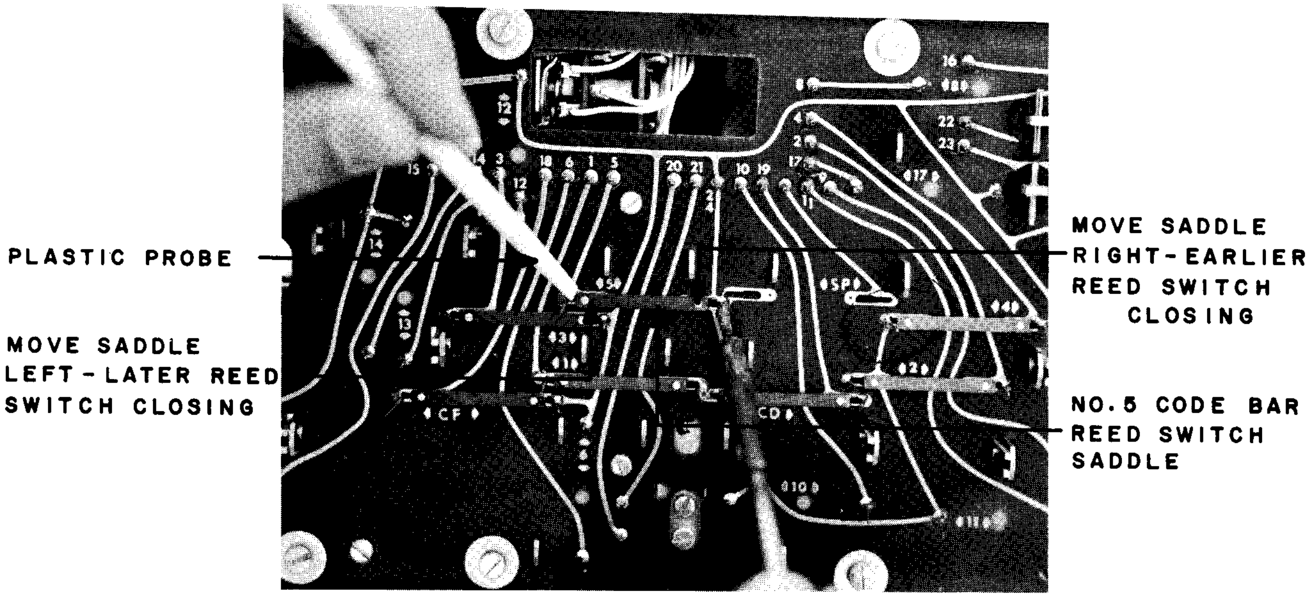

PLASTIC PROBE
MOVE SADDLE LEFT - LATER REED SWITCH CLOSING
MOVE SADDLE RIGHT - EARLIER REED SWITCH CLOSING
NO. 5 CODE BAR REED SWITCH SADDLE
CF
CD

Figure 3-5. Reed Switch Saddle Adjustment

d. Resolder cradle slide in new position, being very careful not to change cradle position.

CAUTION: After making each adjustment, make the final check of that adjustment with the keyboard in a normal horizontal position.

5. CF REED SWITCH ADJUSTMENT

The adjustment of a sequencing function key is to ensure that the lamp on the Tester associated with that key comes on before Common Function (COM FUNC) lamp, and that COM FUNC lamp comes on before bottoming of the key (thus giving overtravel).

To adjust CF Reed Switch proceed as follows:

a. Determine whether CF lamp is lighting early or late.

b. On underside of keyboard, unsolder cradle slide specified CF.

c. Move cradle slide gently to right or left until COM FUNC lamp on Tester just comes on just before function key bottoms. (See Figure 3-2.)

d. Resolder cradle slide in new position, being very careful not to change cradle position.

e. Check that function key has overtravel after COM FUNC lamp comes on.

6. FUNCTION KEY REED SWITCH ADJUSTMENT

a. Determine function lamp that is lighting early or late.

b. On underside of keyboard locate keystem associated with that function.

c. With screwdriver, loosen eccentric cam locking screw (See Figure 3-6)

d. With screwdriver, turn eccentric cam until lamp on Tester specified for that key just comes on at proper position of key travel.

e. Retighten eccentric cam locking-screw, being careful that cam adjustment does not change.

CAUTION: After making each adjustment, make the final check of that adjustment with the keyboard in a normal horizontal position.

7. CODE BAR ADJUSTMENT

The adjustment of the code bars is to limit overtravel in both the operate and retract position. On each end of the keyboard are five limit screws, one on each end for each digit code bar, and one limit screw on one end only for CF and CD code bars.

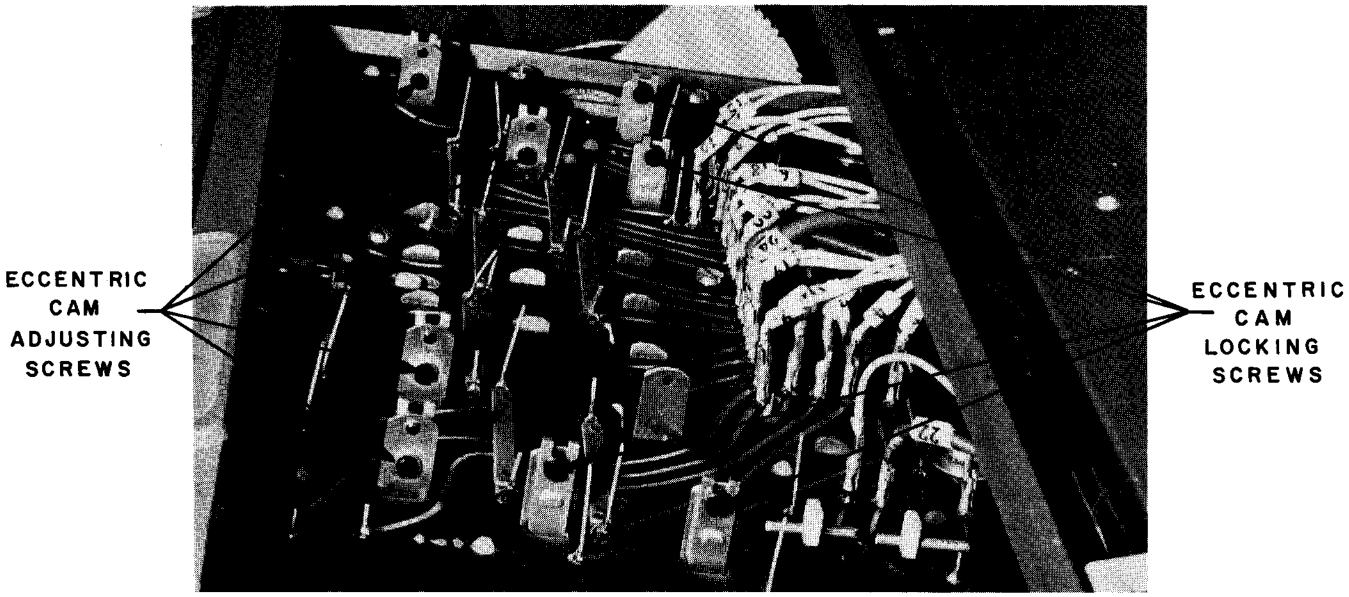


Figure 3-6. Keystem Eccentric Cam Adjustment

a. PRELIMINARY PROCEDURE

(1) Remove Keyboard PC card

(2) Install aluminum test mask

(3) Back off limit screws on each end of the keyboard for 1-5 code bars.

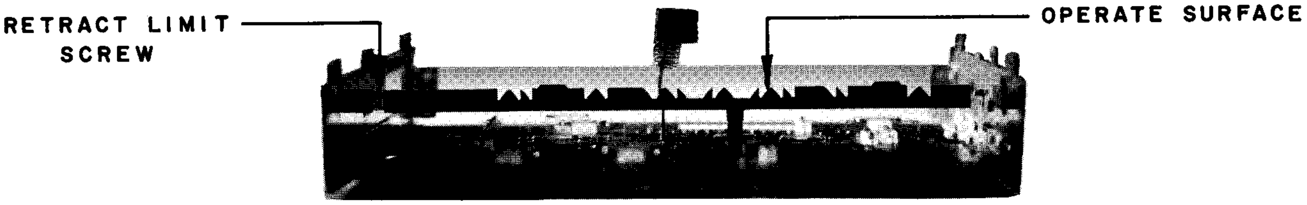
b. DIGIT CODE BAR ADJUSTMENT

(1) Depress digit 5 key, and hold keystem tightly against the test mask with pliers to prevent movement.

(2) Turn each of the five code bar limit screws on the left end of the keyboard in until each screw just touches its respective code bar. (See Figure 3-7.)

(3) Back off each screw 1/8 turn.

CODE BAR RETRACTED



CODE BAR OPERATED

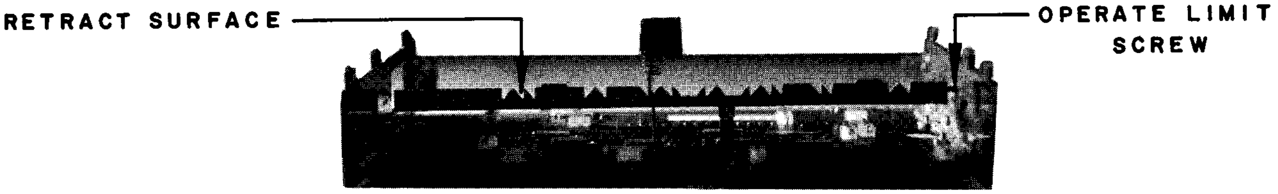


Figure 3-7. Code Bar Limit Screw Adjustment

(4) Depress Zero Key, which brings all digit code bars to retract position.

(5) Turn each of the five code bar limit screws on the right end of the keyboard until each screw just touches its respective code bar. (See Figure 3-7.)

(6) Back off each screw 1/8 turn.

c. CF AND CD CODE BAR ADJUSTMENT

(1) With no key depressed, adjust CD code bar limit screw to just touch CD code bar.

(2) Adjust CF screws just far enough in so that Sign and Repeat keys do not jam.

NOTE: Adjustment of the interlock assembly may necessitate readjustment of CF code bar limit screw.

7. INTERLOCK ASSEMBLY ADJUSTMENT

Improper action of the interlock assembly may be corrected by the following procedure. Replacement of the interlock assembly requires that this adjustment be made.

NOTE: See Section 4 for specific removal and replacement procedures.

a. Remove #2 and #7 keytops (uncovers support bracket screws)

b. Loosen assembly support bracket screws.

c. Remove Keyboard PC board.

d. Install Test Mask.

e. Depress and hold any function key. (This moves CF code bar to operate position).

f. Adjust support bracket so that magnet latch is directly over CD and CF code bar lock notches.

g. Depress latch as shown in Figure 3-8.

h. Adjust support bracket so that latch drops into left edge of notches.

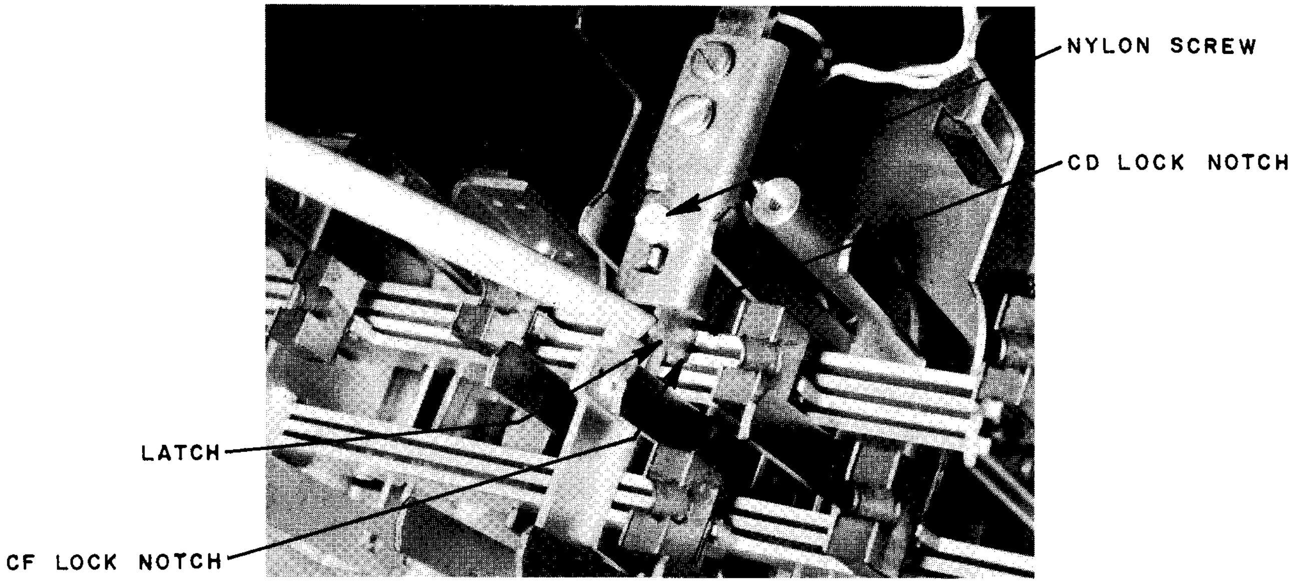
i. Tighten support bracket screws while ensuring that bracket does not change position.

j. Depress and hold any digit key. (This moves CD code bar to operate position.)

k. Check that latch drops into lock notches as in step h. Repeat steps e through i as necessary.

l. With all keys released (CF and CD code bars in retract position), check that latch drops freely into lock notches.

m. If step l is not correct, adjust CF and CD code bar end screws to position right hand notches in line with each other and directly under magnet latch.



NOTE: CF CODE BAR OPERATED

Figure 3-8. Interlock Magnet Latch Adjustment

CAUTION: Turning CF code bar screw too far clockwise can result in Decimal Point key jamming. Turning CF code bar screw too far clockwise can cause insufficient travel of all function keys.

NOTE: The latch release tension adjusting screw (nylon) on top of the assembly will rarely need adjusting. This adjustment should be made only if thorough checking establishes that the cause of slow latch release is lack of return spring tension. Clockwise movement of the nylon screw tightens the spring. Section 4 of this manual contains the setting of this spring upon replacement of the interlock assembly.

C. CHARACTER ADJUSTMENTS

Character adjustments (Figure 3-9) are those adjustments that affect the size of the characters. Character adjustments are: Segment Length (SEG L), Character Width (CHAR W), and Character Height (CHAR H).

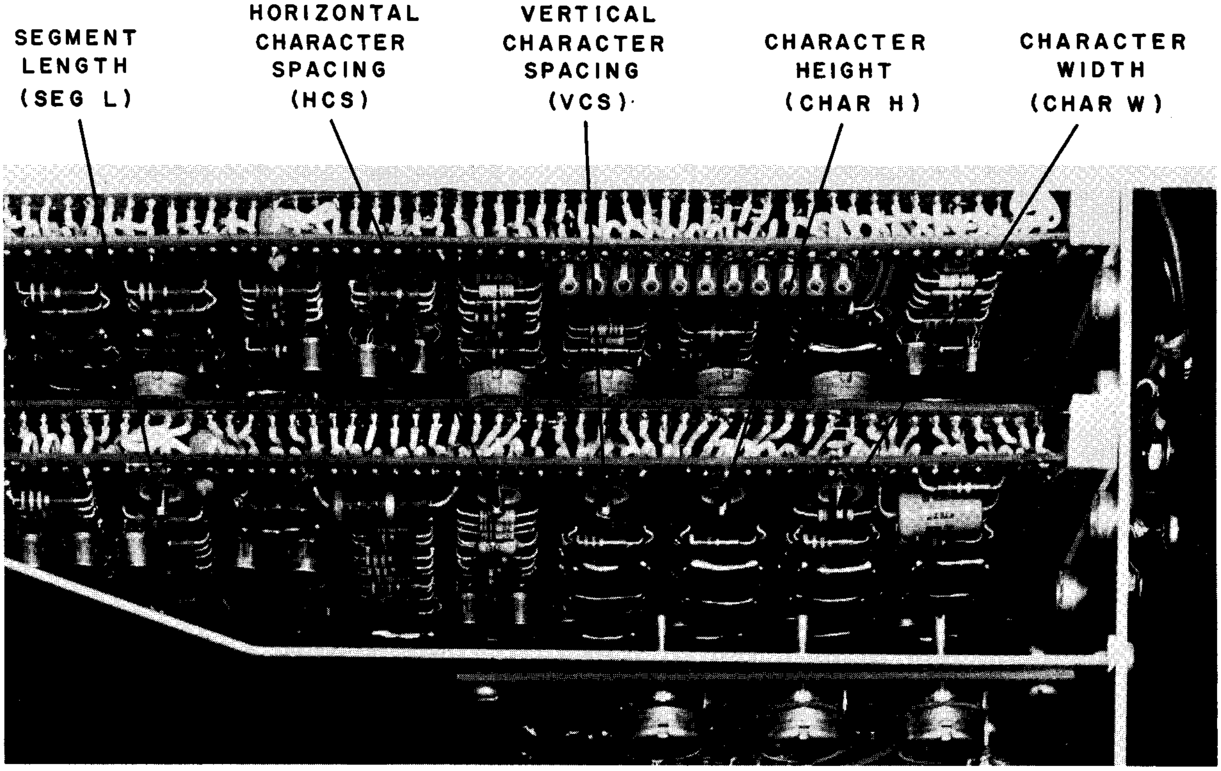

SEGMENT LENGTH (SEG L)
HORIZONTAL CHARACTER SPACING (HCS)
VERTICAL CHARACTER SPACING (VCS)
CHARACTER HEIGHT (CHAR H)
CHARACTER WIDTH (CHAR W)

Figure 3-9. Character Adjustment Controls

1. SEGMENT LENGTH (SEG L)

Segment length adjusts the length of the basic segments and thus the total size of the character. To adjust SEG L proceed as follows:

a. Enter a digit 8.

b. Adjust SEG L until the segments on the Figure 8 character just touch, with no extension or shortening (see Figure 3-10).

2. CHARACTER WIDTH (CHAR W)

Character width (CHAR W) adjusts the total width of a character. To adjust CHAR W, proceed as follows:

a. Enter a digit 8.

b. Adjust CHAR W until the character is approximately the width as shown in Figure 3-10.

3. CHARACTER HEIGHT (CHAR H)

Character height adjusts the total height of a character. To adjust CHAR H, proceed as follows:

a. Enter a digit 8.

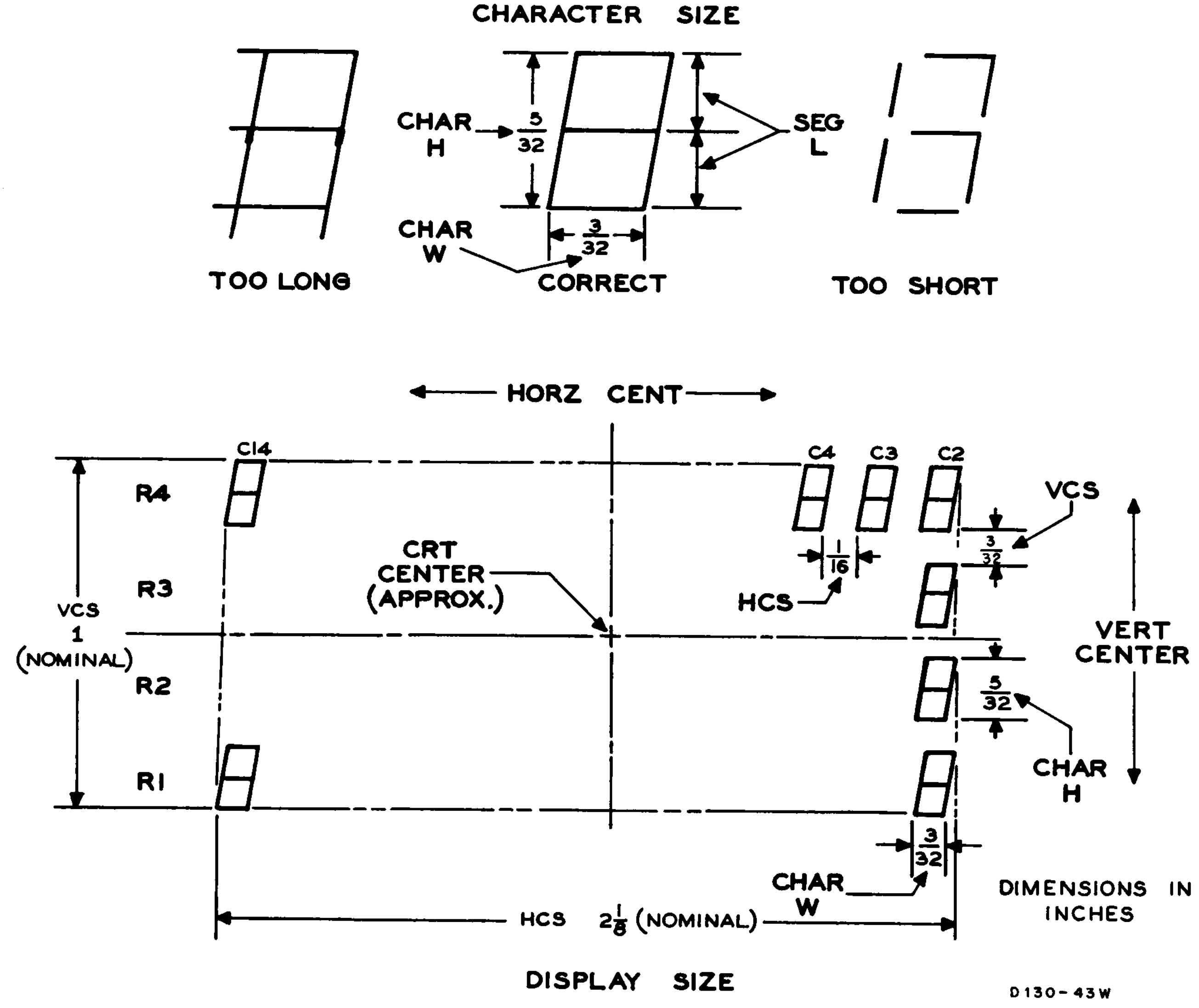


Figure 3-10. Display and Character Dimensions

b. Adjust CHAR H until character is approximately the height as shown in Figure 3-10.

D. DISPLAY ADJUSTMENTS

Display adjustments are those that affect the total appearance of the display from the standpoint of display centering and character spacing. The display adjustments are: Horizontal character spacing (HCS), Vertical character spacing (VCS), Horizontal Centering (HORIZ CENT), and Vertical Centering (VERT CENT).

1. HORIZONTAL CENTERING (HORIZ CENT)

The Horizontal centering control (Figure 3-11) moves the whole display to the right or to the left. To adjust HORIZ CENT, proceed as follows:

a. Rotate HORIZ CENT control until the while display appears approximately centered horizontally on the CRT.

NOTE: HORIZ CENT affects CHAR W. Adjustment of horizontal centering may necessitate readjusting CHAR W control.

2. VERTICAL CENTERING

The vertical centering control (Figure 3-11) moves the whole display up or down. To adjust VERT CENT. proceed as follows:

a. Rotate VERT CENT control until the whole display appears approximately centered vertically on the CRT.

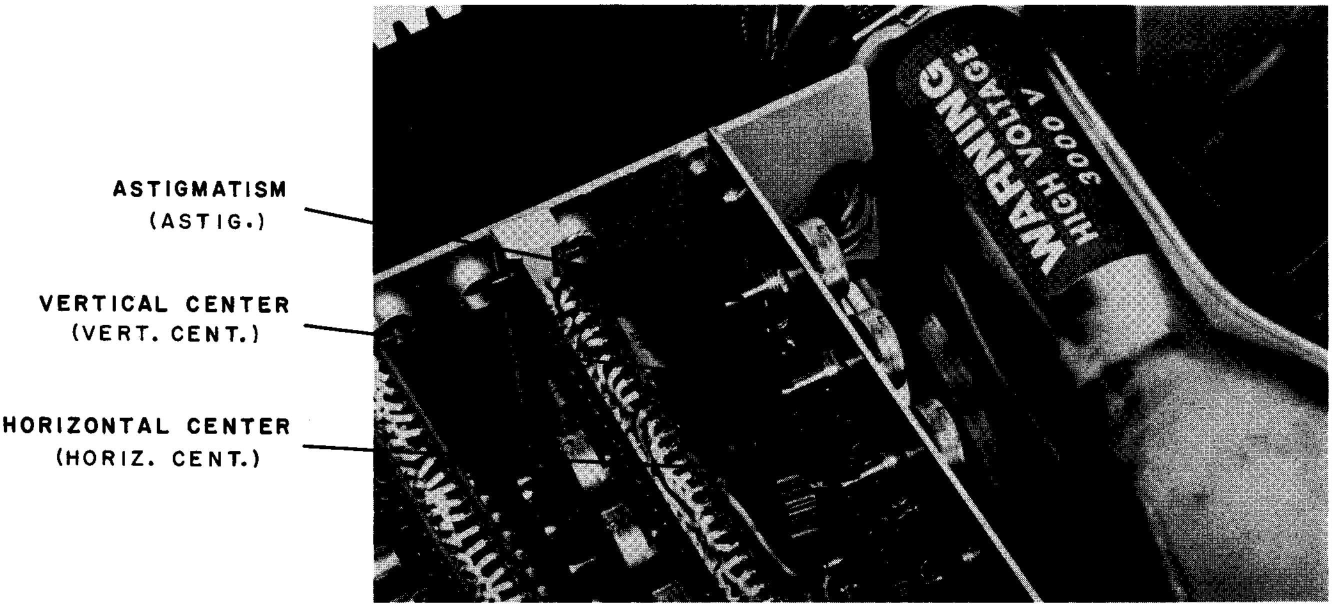


Figure 3-11. Display Adjustment Controls

NOTE: VERT CENT affects CHAR H. Adjustment of the vertical centering may necessitate readjusting CHAR H control.

3. HORIZONTAL CHARACTER SPACING (HCS)

Horizontal character spacing (Figure 3-9) affects the total width of the display, as well as the horizontal spacing between the characters. To adjust HCS proceed as follows:

a. Rotate HCS control until the spacing between the characters is approximately 1/16", and the total width of the display is about 2 1/8".

NOTE: HCS affects HORIZ CENT and CHAR W. These controls should be adjusted alternately for best display.

4. VERTICAL CHARACTER SPACING (VCS)

Vertical character spacing (Figure 3-9) affects the total height of the display, as well as the vertical spacing between characters. To adjust VCS, proceed as follows:

a. Rotate VCS control until the spacing between registers is approximately 3/32", and the total height of the display is about 1".

NOTE: VCS affects VERT CENT and CHAR H. These controls should be adjusted alternately for best display.

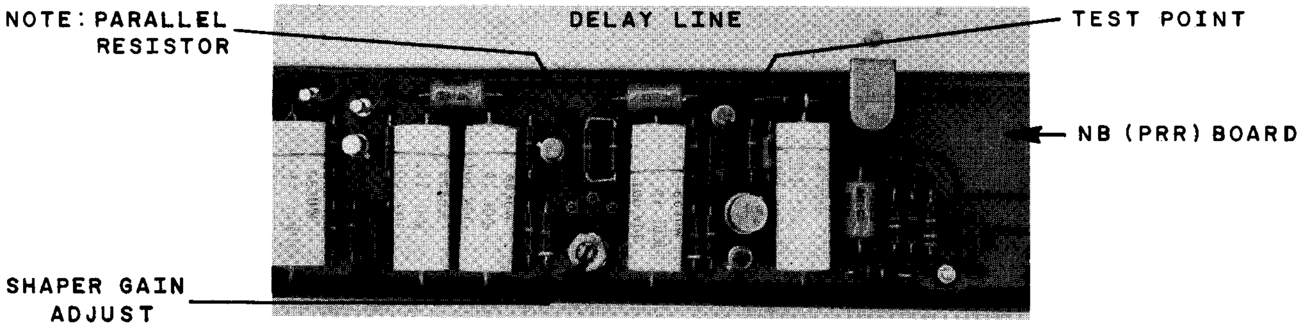


Figure 3-12. Read Amplifier Adjustment

E. READ AMPLIFIER GAIN ADJUSTMENT

Excessive output of the Read Amplifier may result in intermittent changing of numbers on the display. To adjust proper gain, proceed as follows:

1. Remove bottom cover (see Section 4).
2. Place scope probe in test point as shown in Figure 3-12.
3. Check for waveform as shown in Figure 3-13, scope controls as indicated.
4. Loosen lock-nut on Shaper Gain potentiometer.

NOTE: This control is normally glyptoled in manufacture. Once control is broken loose, retightening of lock nut is all that is necessary.

5. Adjust gain for 4 volts (peak) as indicated.

NOTE: In early machines with a high delay line output the gain potentiometer may not be able to adjust output to 4 volts as indicated. In this case, check for 150 ohm resistor paralleling 180 ohm as indicated in Figure 3-12. If resistor is 180 ohms not parallelled, parallel resistor with 150 ohms which will give the necessary range to the potentiometer.

6. Tighten lock-nut securely.
7. Replace bottom cover.

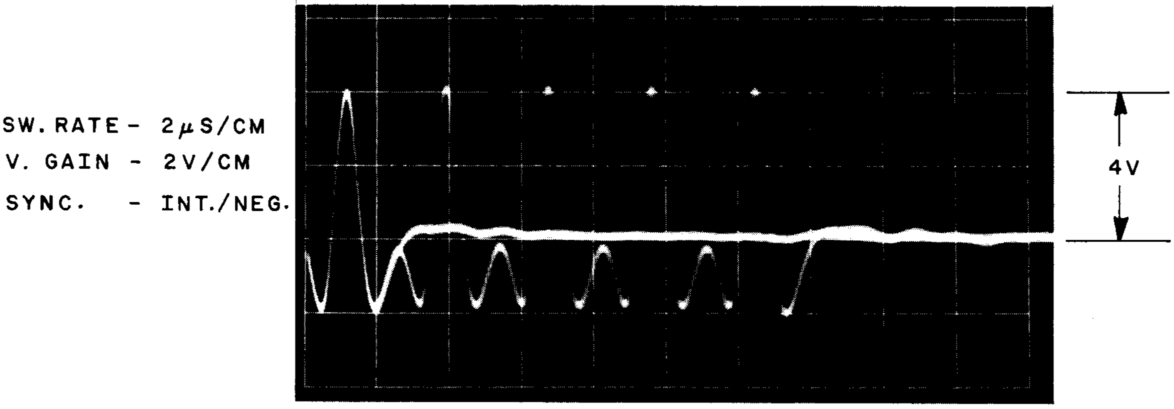


Figure 3-13. Read Amplifier Adjustment Level

KEYBOARD KEYS	COM. DIG.	COM. FUNC.	1	2	3	4	5	DEC. PT.	CLR. ENT.	CLR. ALL	OFL.	RPT.	STORE	RECALL	CH. SIGN	PLUS	MINUS	X	DIV.
0	ON																		
1	ON		ON																
2	ON		ON	ON															
3	ON		ON	ON	ON														
4	ON		ON	ON	ON	ON													
5	ON		ON	ON	ON	ON	ON												
6	ON			ON	ON	ON	ON												
7	ON				ON	ON	ON												
8	ON					ON	ON												
9	ON						ON												
DECIMAL POINT				ON				ON											
CLEAR ENTRY									ON										
CLEAR ALL										ON									
OVERFLOW LOCK											ON								
ENTER		ON			ON		ON												
REPEAT		ON		ON		ON						ON							
STORE		ON		ON			ON						ON						
RECALL		ON		ON	ON									ON					
CHANGE SIGN		ON	ON				ON								ON				
ADD (+)		ON				ON										ON			
SUBTRACT (−)		ON			ON	ON											ON		
MULTIPLY (X)		ON			ON													ON	
DIVIDE (÷)		ON	ON		ON														ON

D130-68

Figure 3-2. Keyboard Tester Lamp Chart

KEYBOARD KEYS								K OHMS BEFORE CF-CD		OUT LINE
0	⊗							∞		
1	⊗		⊗					10.0		
2	⊗		⊗	⊗				5.0		
3	⊗		⊗	⊗	⊗			3.3		
4	⊗		⊗	⊗	⊗	⊗		2.5		
5	⊗		⊗	⊗	⊗	⊗	⊗	2.0		
6	⊗			⊗	⊗	⊗	⊗	2.5		
7	⊗				⊗	⊗	⊗	3.3		
8	⊗					⊗	⊗	5.0		
9	⊗						⊗	10.0		
DECIMAL POINT				⊗				10.0		6
CLEAR ENTRY								∞		8
CLEAR ALL								∞		7
OVERFLOW LOCK								∞		16
ENTER		⊗			⊗		⊗	5.0		
REPEAT		⊗		⊗		⊗		5.0		9
STORE		⊗		⊗			⊗	5.0		14
RECALL		⊗		⊗	⊗			5.0		15
CHANGE SIGN		⊗	⊗				⊗	5.0		17
+		⊗				⊗		10.0		13
−		⊗			⊗	⊗		5.0		12
X		⊗			⊗			10.0		10
÷		⊗	⊗		⊗			5.0		11
	COM DIG	COM FUN	1	2	3	4	5			
	19	18	1	2	3	4	5			
	CODE BAR AND CODE BAR OUTPUT LINES									

Figure 3-4. VOM Adapter Lamp Chart

SECTION 4 - MAINTENANCE

A. SCOPE OF SECTION

This section contains the information necessary to remove and replace certain of the components of the EC-130.

B. LIST OF MAINTENANCE TOOLS

1. NORMALLY AVAILABLE TOOLS

a. Dusting Brush	T18483
b. Cleaning Brush	T18071
c. Diagonals, 6"	T1811
d. Long Nose, 6"	T18424
e. Screwdriver, 1/4" tip	T18106
f. Pliers, Gen. Purpose	T18182
g. Screw Starter	T18284

2. SPECIAL TOOLS

a. Plastic Probe	T18464
b. Card Extractors	T18482
c. VOM - Triplett 310	T18082
d. Softip Hammer	T18076
e. Hex Setscrew Wrench	T18039
f. Tweezers	T18328
g. Oscilloscopes - Tektronix 535, 422, 310A	
h. Keyboard Tester, or Keyboard Test Adapter for VOM	
i. Soldering Iron, 15W	T18702
j. Solder (1 lb.)	T18704
k. Soldering Iron Tip	T18703
l. Spring Hook	T18461

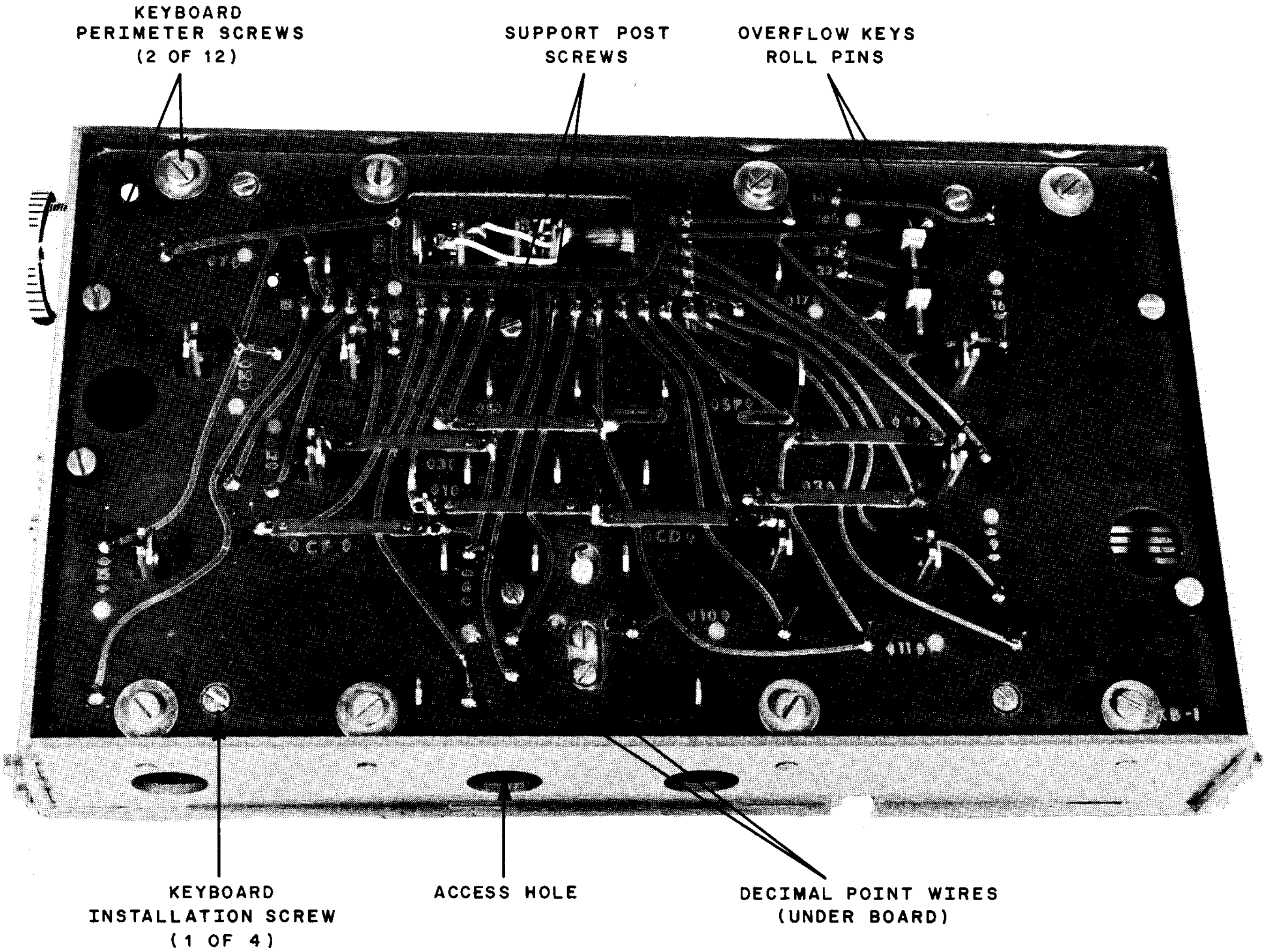

KEYBOARD PERIMETER SCREWS (2 OF 12)
SUPPORT POST SCREWS
OVERFLOW KEYS ROLL PINS
KEYBOARD INSTALLATION SCREW (1 OF 4)
ACCESS HOLE
DECIMAL POINT WIRES (UNDER BOARD)

Figure 4-1. Keyboard Mask

C. KEYBOARD MAINTENANCE

The keyboard is a precise electromechanical device. In order for the keyboard to function satisfactorily, maintenance must be done carefully. In all of the maintenance routines mentioned, carefully follow step by step procedure.

1. KEYBOARD MASK REMOVAL

NOTE: Use a calculator pad to prevent keytop damage.

a. REMOVAL - Refer to Figure 4-1.

(1) Remove the perimeter screws (12).

(2) Remove the rollpins (2) and the rubber washers from the overflow key.

(3) Remove the support post screws.

(4) Remove the D.P. wires (2) from the pin connections on the under side of the keyboard mask.

CAUTION: The wires should be drawn out of the access hole to prevent jamming the Decimal Point key, or breaking the D.P. reed switch. The dangling wires also serve as a reminder that they are not connected when the keyboard is reinstalled.

(5) Lift out keyboard printed circuit mask.

NOTE: If the keyboard is now turned over, the keyboard installation screws will fall out. This is of no consequence, but do not leave them out upon replacement.

b. REPLACEMENT

(1) Replace keyboard installation screws in grommeted holes, and check cleanliness of keyboard, i.e., no small metal washers and springs, or over-greased code bars.

(2) Fit PC mask over keystems.

NOTE: Fit the mask first over the function keystems; enter keystem; and then the digit group. (D.P. and 0 keystems, along with Clear Entry and Clear All, will be somewhat of a problem.)

(3) Install screws in support posts.

NOTE: The mask position can vary slightly which may change electrical operation. Also, some binds may be removed by allowing the mask to "settle" before completely tightening any of the screws.

(4) Replace the perimeter screws.

(5) Replace the Overflow key washers and roll pins.

CAUTION: Be sure to grasp the wire connectors with the pliers carefully to avoid damaging the connectors.

(6) Reconnect the D.P. wires to the pins, using needle nose pliers.

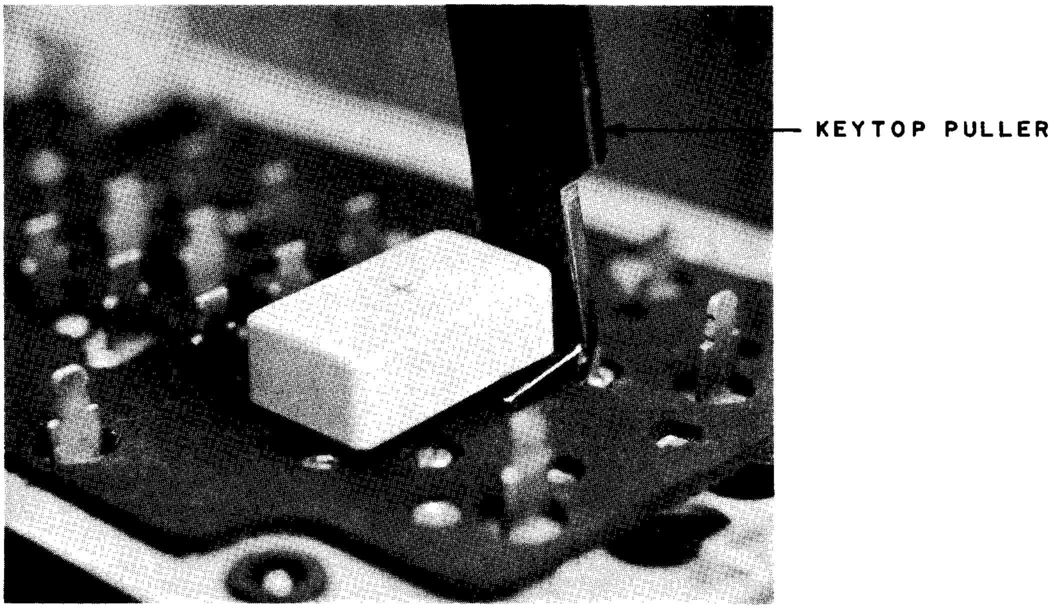


Figure 4-2. Keytop Removal

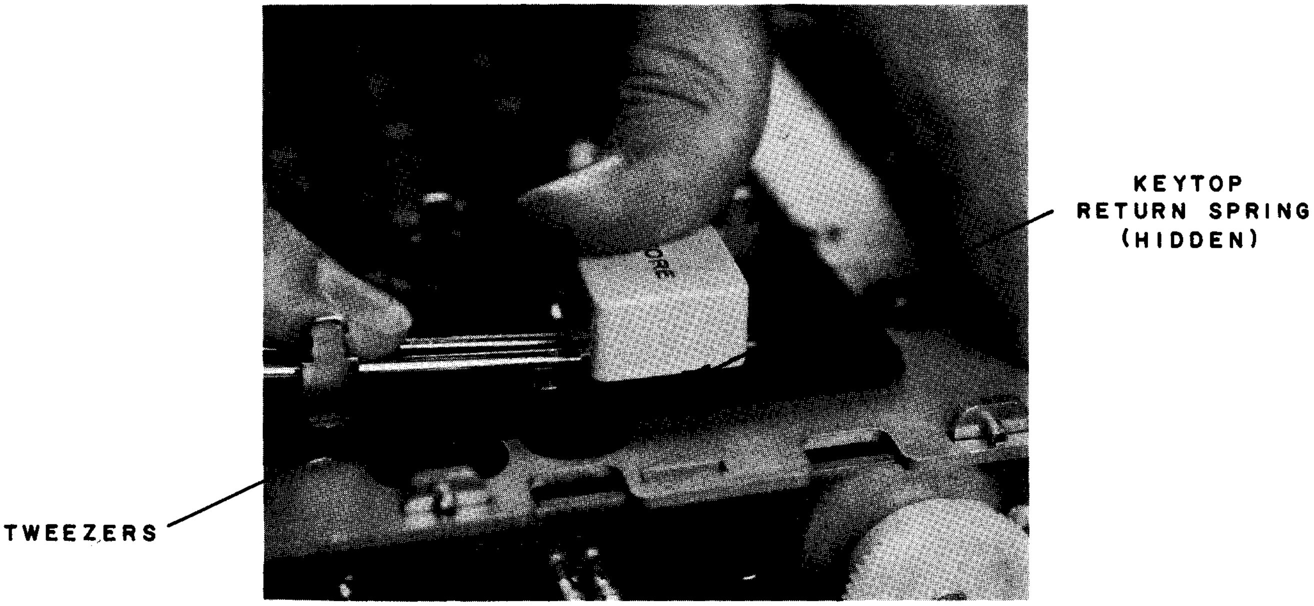


Figure 4-3. Keytop Replacement, Preliminary

2. KEYTOP REMOVAL AND REPLACEMENT

Keytops are best removed with the aid of a keytop puller. Proper application of the puller (see Figure 4-2) insures that each keytop is removed with a minimum of strain or stress to the keystem guides and keyboard mask. Adjacent keytops may be damaged on the sides when a keytop is removed if the offset slot in the keytop puller is not used in the removal of 1-3 and 7-9 keytops.

When replacing keytops, a new keytop for each assembly is required because upon removal the "Mae West" design of the keystem destroys the locking action of the keytop.

Press the keytop on firmly using a suitable support for the keystem. Be sure to depress the spring under the keytop with tweezers to prevent it from becoming damaged. (See Figure 4-3).

After the initial fitting of the keytop, use a plastic-headed mallet and drive the keytop on, using a firm support under the keystem. (See Figure 4-4.)

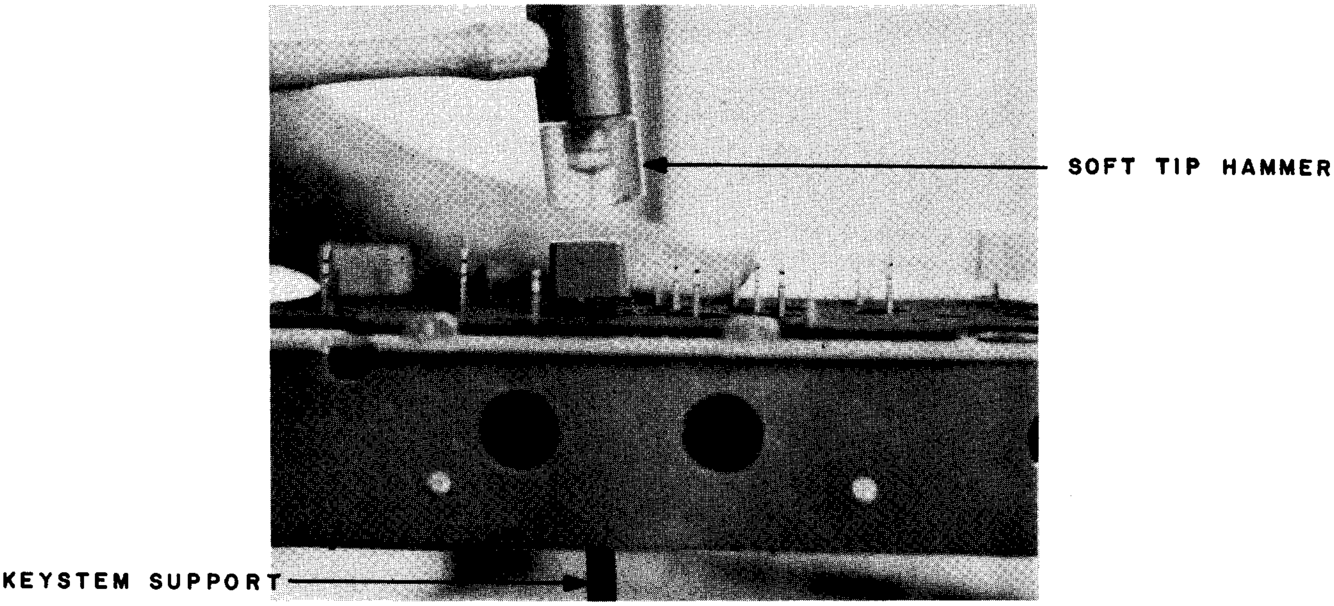


Figure 4-4. Keytop Replacement, Final

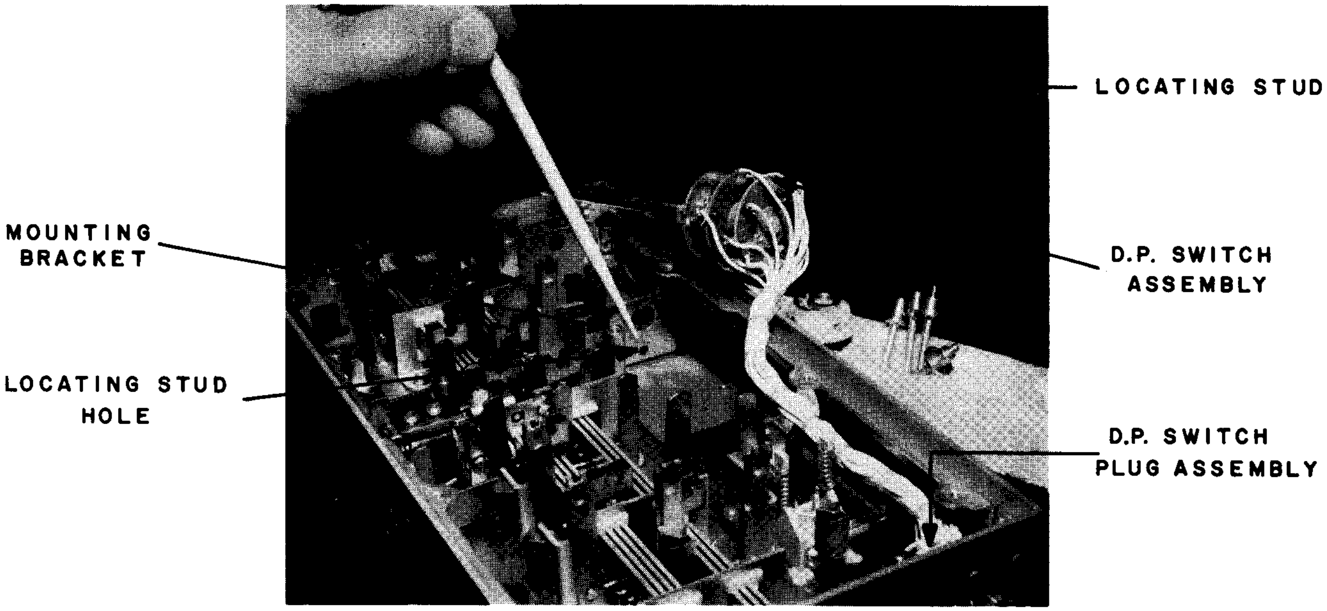


Figure 4-5. Decimal Point Switch Replacement

3. DECIMAL POINT SWITCH REPLACEMENT

a. REMOVAL - Refer to Figure 4-5.

(1) Remove keyboard PC mask.

(2) Remove gear from shaft of decimal point switch (Allen head setscrew.)

(3) Remove screws in holding D.P. plug assembly.

(4) Remove nut holding D.P. switch assembly to bracket.

(5) Remove switch assembly.

b. REPLACEMENT

(1) Insert new switch assembly.

CAUTION: Be sure to put stud on switch assembly into hole in mounting bracket. (See Figure 4-5.)

(2) Replace nut holding switch assembly to bracket.

(3) Replace D.P. plug assembly, and install and tighten screws.

(4) Replace decimal point gear on switch shaft. Tighten Allen head setscrew.

(5) Replace keyboard PC mask.

(6) Check keyboard functional operation.

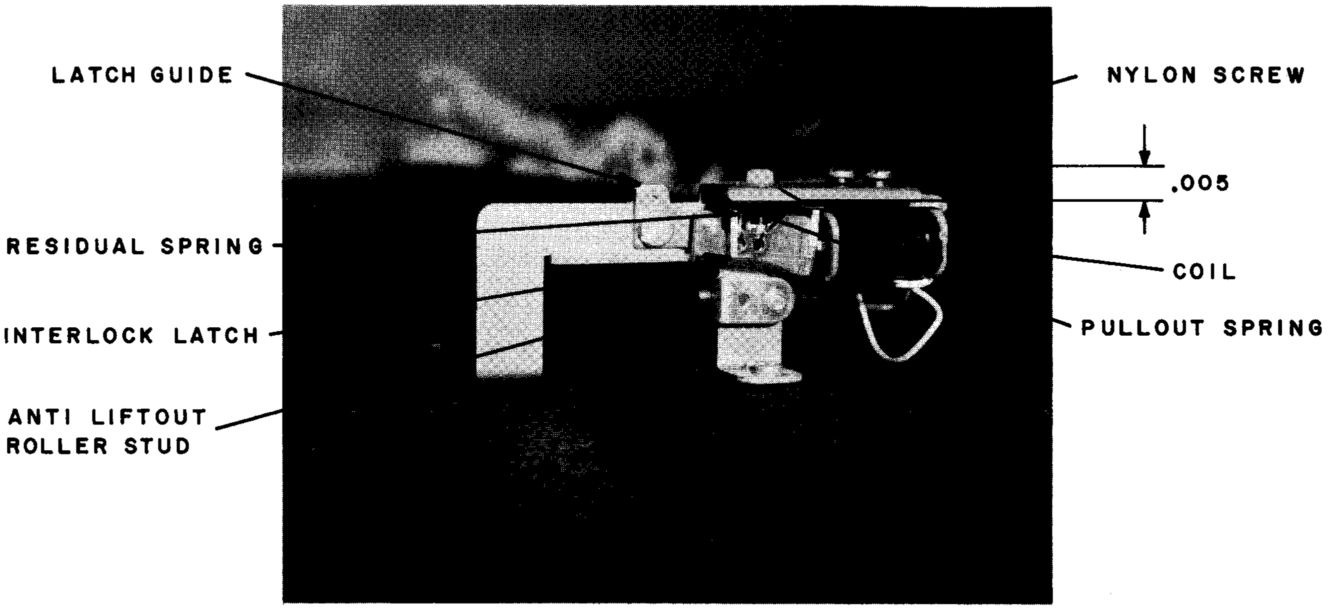


Figure 4-6. Interlock Assembly Adjustment

4. INTERLOCK ASSEMBLY ADJUSTMENT

a. Clearance between the anti-liftout roller stud and CF code bar should be .002", this allows free movement laterally of the CF code bar. The roller stud bracket should always be assembled in the manner illustrated in Figure 4-6. (Digit keystem binds occur with the reversal of the roller stud plate and screw.)

b. The interlock latch guide prevents lateral movement of the latch allowing accuracy in the interlock adjustment (See Section 3). The guide also has a window through which the interlock latch stud moves when the coil is energized. The latch guide is positioned to allow a small (.001) air gap between the latch plate and coil core with coil energized.

c. The residual spring holds the latch in the restored position. The magnet coil, when energized, works against the tension and mass of the interlock latch. The pullout spring aids in restoring the operated latch in the event of a latch bind caused by retract pressure offered by CF spring on the CF code bar. The nylon screw is unscrewed enough to allow the pull-out spring to be picked up in the middle of the interlock latch travel when the coil is energized. This adjustment allows a slack gap of approximately .005" when measured from under the nylon screw head to the interlock bracket frame.

NOTE: Check code bars for binds by manually moving each one. Notice relation of brackets to code bars. It is easiest to insert code bars in the brackets if the set is assembled upside down on a calculator pad beforehand. Also, the code bar bearing surface can be seen for alignment. After code bars 1, 2, 3, and 5 are installed in bracket A, insert code bar 4 in bracket B and finish assembly. Bracket C, the smallest, is installed last.

(2) With tweezers, insert CD and CF code bar retract springs.

(3) Install code bar brackets, and screws.

(4) Replace interlock bracket.

(5) Install test mask.

(6) Adjust interlock (See Section 3).

(7) Remove test mask.

(8) Install keyboard printed circuit mask.

(9) Check keyboard functional operation.

5. CODE BAR ASSEMBLY REPLACEMENT

a. REMOVAL - Remove the keyboard from the machine and remove the following parts in sequence. The relationship of the code bars to support brackets can be seen in Figure 4-7.

(1) Keyboard Printed Circuit Mask (Screw locations on Figure 4-1).

(2) Digit 2 and Digit 7 keytops.

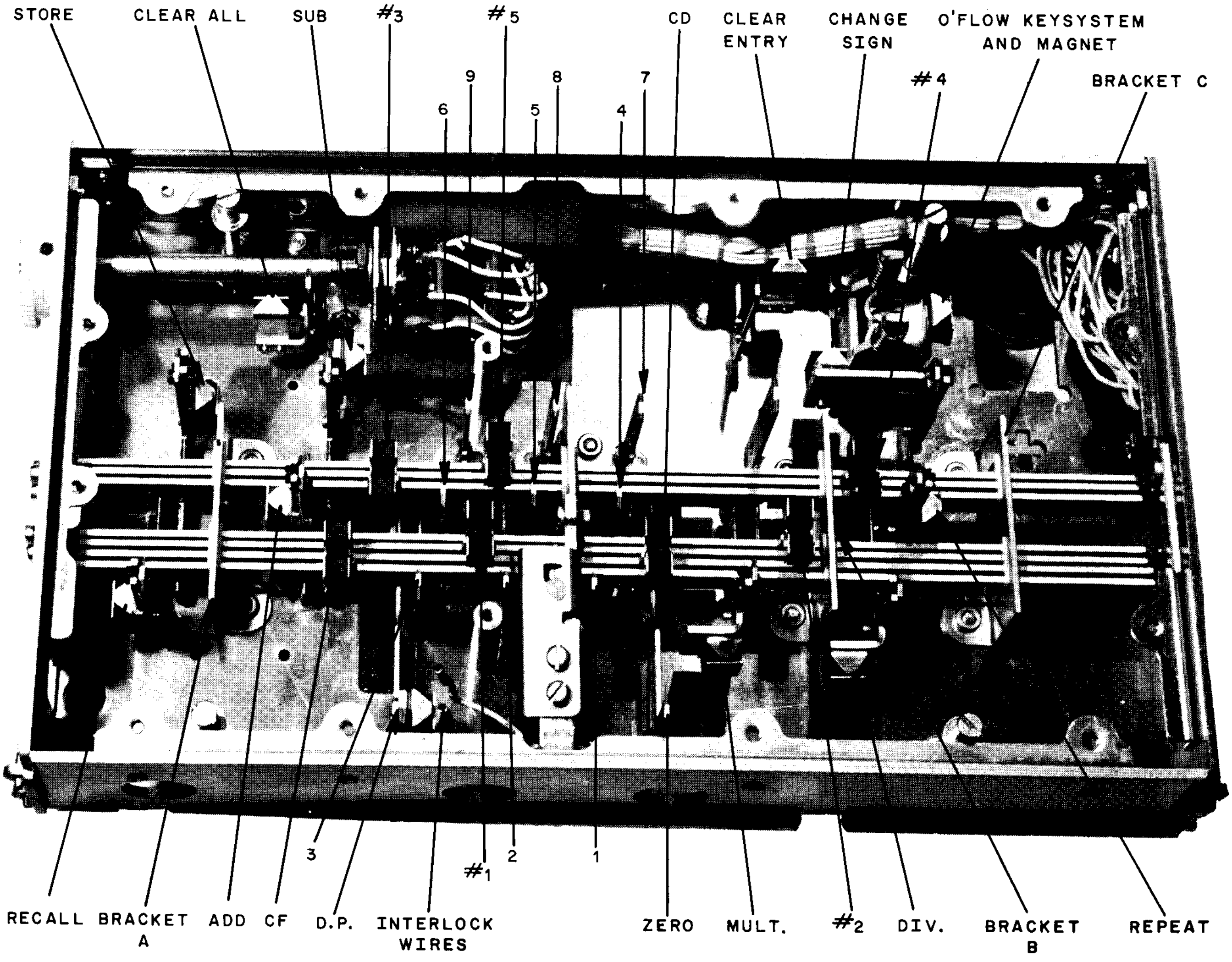


Figure 4-7. Keyboard Inner Parts Placement

(3) Interlock bracket screws.

(4) Interlock bracket.

(5) Remove CF and CD code bar retract springs.

(6) Remove code bar bracket screws.

(7) Remove old code bar set from keyboard.

b. REPLACEMENT

(1) Install new code bar assembly into keyboard.

6. CODE BAR IDENTIFICATION

The Code Bar Identification drawing (Figure 4-8) will aid in identification of each of the seven code bars installed in the keyboard.

a. To identify #1, #2, #3, #4, or #5 code bar,key the code bar alongside the CD code bar. The diagonal keystem striking surface indicates which way the code bar will move when a keystem strikes the diagonal. Note that certain of the striking surfaces are diagonal both ways. In that case, depression of a digit key moves the code bar one way to operate position, while depression of another digit key can move the code bar the opposite way to a retract position. (See Keyboard Function discussion.)

b. Noting which keystems move the code bar to operate position tells indirectly which code bar is being identified. Realizing that if the code bar is operated when a digit 3 is depressed, the code bar must be number 1, 2, or 3, each of which is operated by digit 3 key. If there is an operate surface in line with the digit 2 keystem, the code bar could be #2 code bar. Next, if there is a retract surface in line with digit 1 keystem, logically the code bar is #2 since #1 key retracts #2 code bar.

c. An alternate method of code bar identification is to measure the shortest distance from one end of the code bar to the magnet support. Measurements are as follows:

#1 Code Bar	-	3 7/16"
#2 Code Bar	-	2 15/16"
#3 Code Bar	-	2 9/16"
#4 Code Bar	-	3 5/8"

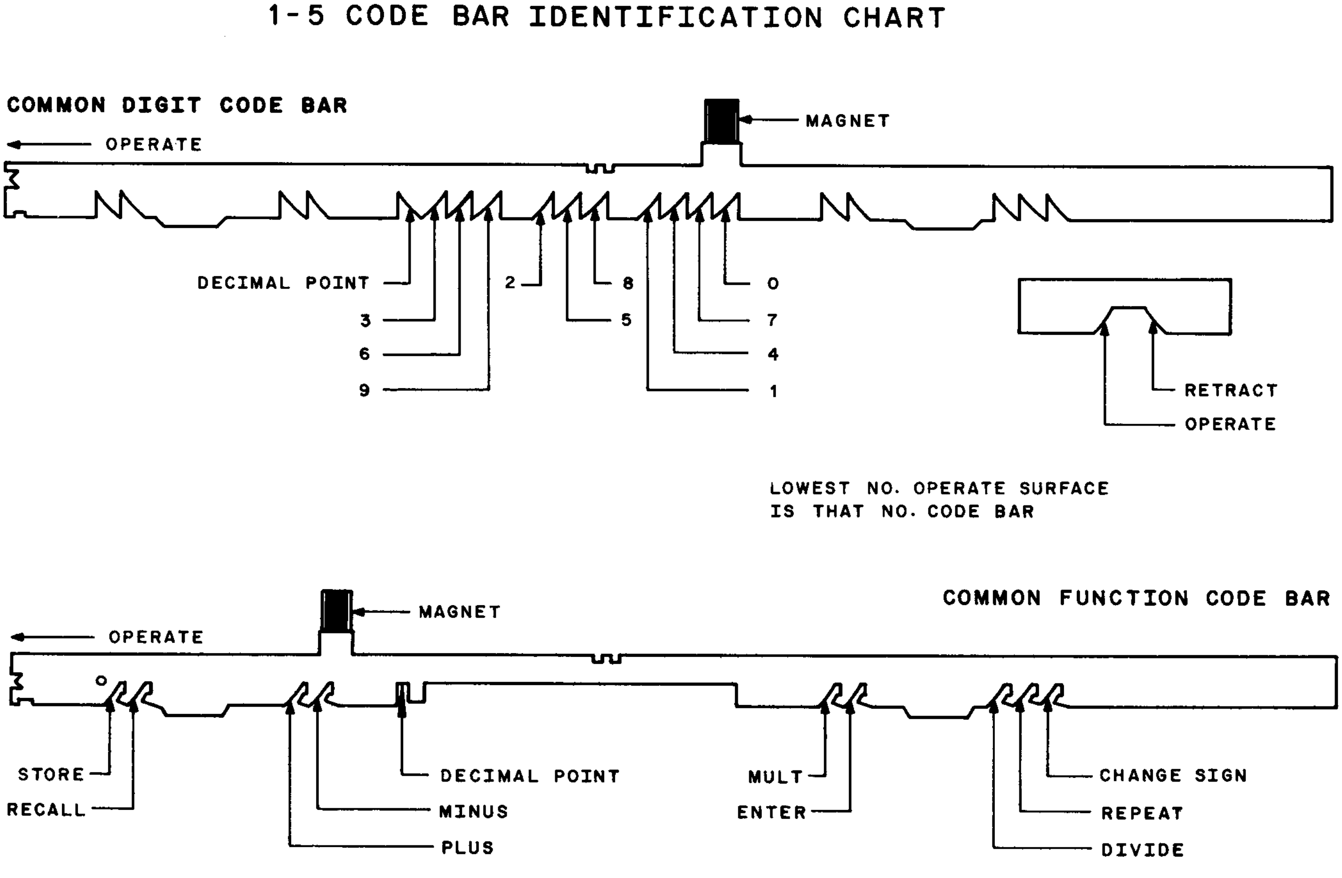


Figure 4-8. Code Bar Identification Chart

7. KEYSTEM IDENTIFICATION

The Keystem Identification illustration (Figure 4-9) will aid in the identification of the keystems installed in the keyboard.

a. Clear All and Clear Entry are similar, but Clear Entry will not clear the D.P. switch shaft, thus they are not interchangeable.

b. Plus (+) and Multiply (X) keys are similar but not interchangeable.

c. Extreme care should be used to prevent interchanging similar keys. Attention to detail and reference to the keyboard PC mask will prevent this.

8. KEYBOARD TOP INSTALLATION

A production change to the keyboard top may necessitate changing the keyboard top presently in the field with a new type keyboard top. At the same time, the new digit 4, 5, and 6 keystems must be modified by removing 1/16" off the crown to keep these keys to the same level as the rest of the digit group. The new, modified digit 4, 5, and 6 keystems are installed at the same time as the keyboard top. Also, Add (+) and Repeat keystems must be changed to a new type.

To install a new keyboard top, proceed as follows - Refer to Figure 4-10.

a. Install aluminum test mask.

b. Remove Clear All keytop.

c. Remove screws (2) on D.P. switch bracket. (See Figure 4-10.)

d. Remove Clear All keystem and label for reinstallation.

e. Remove screws (3) from keyboard-top retaining bracket.

f. Remove roll pins (9) from keyboard top.

g. Remove remaining keytops except for Overflow Key.

NOTE: Work from the outside in.

h. Remove remaining keystems, and label for reinstallation.

i. Remove support post screws. (See Figure 4-10.)

j. Remove keyboard top. (Pry evenly along the edge of the keyboard frame.)

k. Remove screws (2) holding magnet to Overflow keystem assembly.

l. Remove Overflow assembly.

m. Peel the sponge mat off the old keyboard top and re-apply with contact cement to new keyboard top.

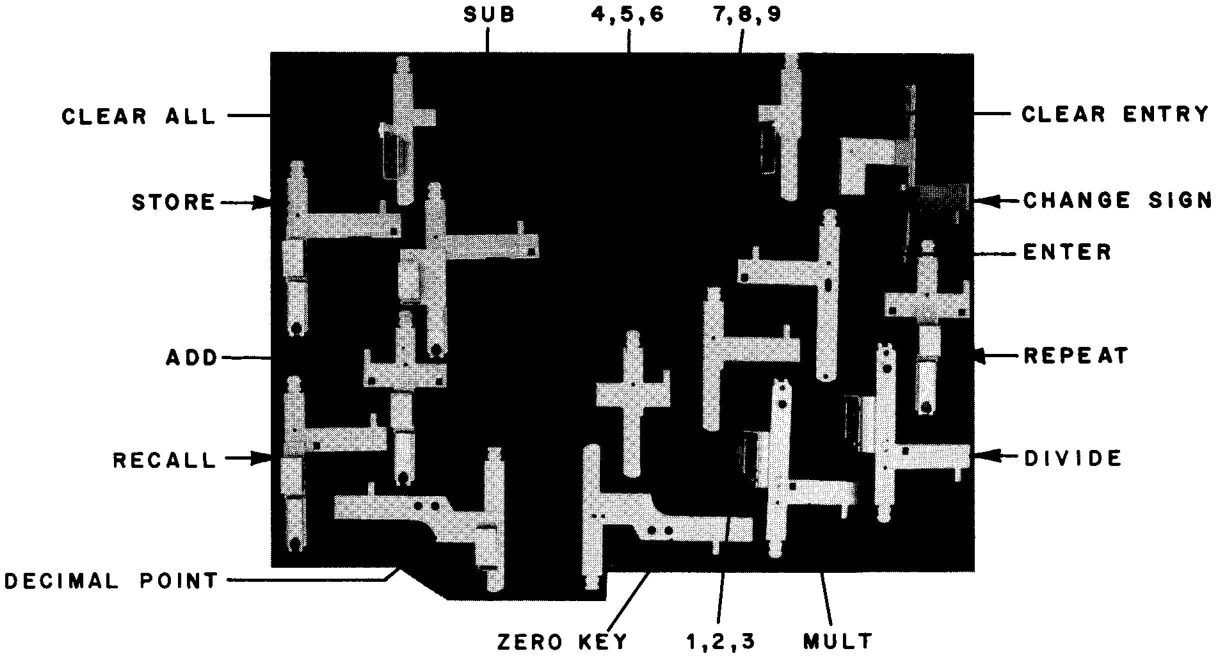


Figure 4-9. Keystem Identification

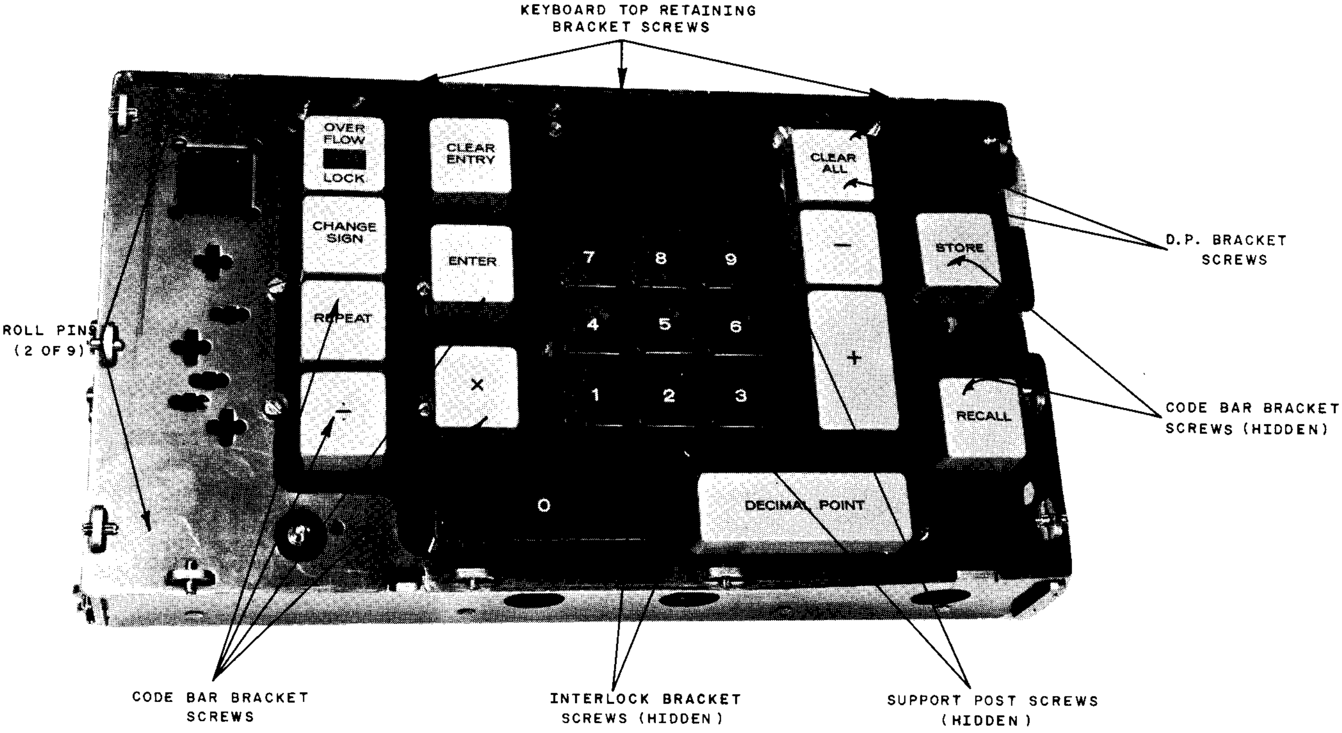


Figure 4-10. Keyboard Top Installation

n. Remove support posts and reattach to new keyboard top.

o. Remove digit key supports and discard. (Supports are not needed in new assembly.)

p. Remove digit keystems.

q. Remove rubber underboard pads and reapply to new keyboard top (Model Cement will be satisfactory. Trim pads as necessary to fit new top.)

r. Install new paper for D.P. switch wafer insulation.

s. Reinstall Overflow key assembly, and reattach magnet. (Refer to step k.)

t. Replace new keyboard top in position, and secure with roll pins and bracket screws. (Refer to steps e and f.)

u. Reinstall Clear All keystem. (Refer to step d.)

v. Reinstall and tighten screws on D.P. switch bracket. (Refer to step c.)

w. Replace remaining keystems.

x. Replace code bar assembly and fasten code bar brackets.

y. Replace CF and CD code bar retract springs. (Tweezers will be helpful.)

z. Replace interlock bracket. (CF and CD code bars may be flexed slightly to ease installation.)

aa. Install aluminum test mask.

bb. Replace key tops.

cc. Check keyboard mechanical action.

dd. Adjust interlock action.

ee. Remove aluminum test mask and replace with keyboard PC mask.

ff. Check keyboard electrical function.

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A. INTRODUCTION

This article is written as a primary training device and presupposes a thorough understanding of the detailed logic of the EC-130 Calculator. It is intended that the student, using only this article and the associated block diagram, will be able to grasp both the logic and the circuitry of this machine by drawing upon his background of training and experience on the EC-130 Calculator.

Because this is not a new machine but a redesign of the existing EC-130, many basic circuits are identical or nearly identical to existing circuits in the EC-130. These areas will be passed over lightly or not touched upon at all. This will limit the subject to the differences in logic and circuitry between the Three Counter EC-130 and Four Counter EC-130. This limitation has two advantages. First, it reduces the size of the volume to a small package of vital information and, second, it avoids the discouragement which normally accompanies the thought of plowing through a massive volume of already familiar information to find the desired information.

B. THE ENTRY ENCODER

The Entry Encoder is a scale of eight binary counter which has only parallel inputs and parallel outputs. It consists of three flip-flops, and replaces the Change Sign, Shift Down, Store, Recall, Repeat, and Add or Sub flip-flops. The Entry Encoder is used in the Change Sign, Clear Entry, Store, Recall, Repeat, Add, and Subtract functions, and the appropriate keyboard switches are used to set the Entry Encoder flip-flops. The keyboard is the same as the one used in the Four Counter machine so there are necessarily some changes in the keyboard interface to permit one switch to set the proper binary code into the Entry Encoder. The enclosed Encoder Truth Table (Figure 5-1) shows which Encoder flip-flops are set by each of the seven keyboard switches listed. The Encoder flip-flops are reset after each function so it is not necessary to reset any flip-flops with a keyboard switch. It is necessary only to set the appropriate flip-flops; however, because each flip-flop can be set by more than one switch, the switch outputs are applied to the flip-flops through diode OR gates. For example, the EEN2 FF can be set by the Change Sign switch, the Repeat switch, and the Store switch. These switch outputs are applied to an OR gate, and the output of the OR gate is integrated to provide the DC enable signal for the AC AND gate which sets the EEN2 FF.

ENTRY ENCODER TRUTH TABLE

FLIP-FLOP	1	2	4
RECALL	1	0	0
CHG SIGN	0	1	0
REPEAT	1	1	0
CLEAR ENTRY	0	0	1
ADD SUB	1	0	1
STORE	0	1	1

Figure 5-1

Note, also the connection between the Add switch and the Subtract switch. This connection exists for the same reason as on the Four Counter machine. The Subtract switch must enable the Sign Control FF to be reset and the Add switch must not, but both switches must enable the EEN1 FF and the EEN4 FF to be set. Hence, a diode is connected to isolate the two switches in one direction and connect them in the other direction. The Clear Entry switch is not used as an input to the OR gate which sets the EEN4 FF because the output of the Clear Entry switch must be used to reset the Overflow FF as well as to set the EEN4 FF; whereas it is not desired to have the outputs of the Add, Subtract, or Store switches enable the resetting of the Overflow FF.

The Encoder is reset at the end of each function by ERF3 (the same signal which resets the function flip-flops in the Four Counter machine).

C. THE TIMING CHAIN

There are a few changes in the timing chain, but all are relatively simple. The emitter followers have been removed from the set outputs of the D, E, F, and G flip-flops because there is insufficient loading of these signals to warrant the additional drive. The P flip-flop has been eliminated and R1 will not be intensified.

The clock flip-flop has been eliminated, and the output of I-169 is used as the clock signal and triggers the A flip-flop. Since the clock frequency must stay at about 333KC, the master oscillator frequency is cut in half by using .0056 µf and .0033 µf capacitors in the tank circuit in place of the 1500 pf and the 820 pf capacitors. The emitter follower and the inverter in the oscillator circuit have also been changed to provide the risetime and falltime necessary for the clock signal. The new oscillator circuit is shown in Figure 5-2.

An extremely important point to remember is that the A, B, and G flip-flops are still preset so that the sync pulse ALWAYS comes off the delay line in B3 R3 C0 time. This is true irregardless of the position of data in the delay line with re-

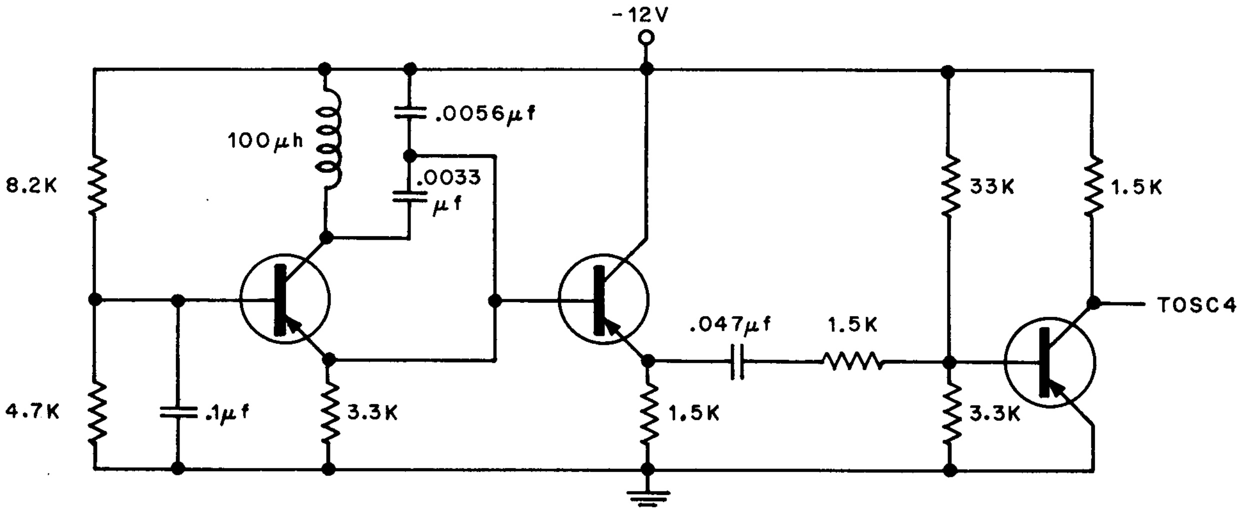

Figure 5-2

spect to the sync pulse. (This is also true in the Four Counter machine but this point bears re-emphasizing.) Much will be made of this later.

Two other changes involve the decoded timing signals. Since TC04 is needed as well as TC03, TC03 is now an input to an inverter (I-301) to generate TC04. Also, C15 is no longer developed as a separate signal. So the OR gate that develops TCX5 (I-229) has four timing signal inputs which define C15 time. The same signals are also used at two other OR gates to define C15 time. All in all, the timing chain has not been changed much.

D. THE PHASE COUNTER

Only one very small change has been made in the Phase Counter. Since MIAD3 is no longer developed, MSU3 is used to inhibit stepping the counter to PS6 from PS5 in divide. This will also inhibit stepping from PS4 to PS5 so an AC AND gate is used to set the PC1 FF in PS4 of divide. AC AND gate 1171 is enabled by MSU3 and HOME1 is the trigger. So, when the Phase Counter is in PS4 of Divide A-1171 enables HOME1 to step the counter to PS5, but does not enable it to be stepped to PS6 until MSU3 is lost. This poses an interesting question. Is MSU3 detrimental to the operation of the counter in subtract? No, it is not, because MSU3 is not developed until PS7 of subtract, and although MSU3 inhibits stepping the counter to PSZ, PS73 and HOME1 reset the CF FF and the Phase Counter is pulled to PSZ by the override reset.

PSZ3 is no longer decoded because it is no longer needed.

E. DATA FLOW

1. NORMAL DATA FLOW

In this machine, data flow in machine idle is serial from the delay line to the A Counter, parallel from the A Counter to the C Counter, and serial from the C Counter to the delay line. Hence, "normal" data flow uses only two counters instead of three as in the Four Counter machine. The B Counter has been eliminated in this machine.

2. SHIFT LEFT

Elements 121 and 122 actually enable SAD9 to be generated, and elements 128 and 129 actually enable SDC9 to be generated. To enable SAD9, one of the inputs to OR gate 121 must be logic 1 (0 volts). To enable SDC9, one of the inputs to OR gate 128 must be logic 1. The inputs to these two OR gates come from Inverters I-094, I-101, I-096, and I-105. I-105 will not be discussed because the logic used to complement R1 is the same in both machines. To enable SAD9 in Recall or Repeat, the output of I-094 must be logic 1, so the input to I-094 must be logic 0 (negative). The output of AND gate 093 will be negative when any input is negative. To enable SDC9 in Recall or Repeat, the output of I-096 must be logic 1, so the input to I-096 must be logic 0. The output of AND gate 093 will be negative when any input is negative. The development of SAD9 and SDC9 to shift left, shift up, and shift down is controlled by I-101. To enable SAD9 and SDC9, the output of I-101 must be logic 1, so the input must be logic 0 (negative). This will occur when any input to AND gate 100 is negative.

In further description of the logic to enable SAD9 or SDC9 to be developed, the signal will be considered developed when an input to AND gates A-093, A-100, or A-092 has been proved to be negative.

a. DIGIT ENTRY. Shift left is done the same as in the Four Counter machine. For example, in a digit entry, OR gate 060 and Inverter 061 develop MEIL3 which develops M1L4. M1L4 is an input to OR gate 097 to develop SAD9 and SDC9 at the end of R1 time.

b. DECIMAL ALIGN. Align shift R1 left is developed the same way as entry shift R1 left except that OR gate 053 and inverter 054 develop MAIL3 which develops M1L4.

c. ENTRY AND ALIGN SHIFT LEFT OVERFLOW. If an overflow occurs in entry or align shift R1 left, the overflow is determined by AC AND gate 1224 at the input of the Overflow flip-flop. CDZ4 is the DC input, and ECD2 is the AC input. If there is a digit other than zero in R1 C14, and another digit is entered into R1, then the digit that was in R1 C14 is shifted into D at B15 R1 C14 time in PS7 and no more SAD9 pulses are generated. So the digit stays in the D Counter and is there when HOME1 resets the Common Digit flip-flop. ECD2 transitions positive and sets the Overflow flip-flop. If there is an overflow in align shift R1 left in PS1, it is necessary to terminate the function at the end of PS1. If the function were allowed to continue with an overflowed number, errors could develop. If there is an overflow in PS1 of a function AC AND gate 1103 resets the Common Function FF at the end of PS1. If the overflow FF sets in PS1, AOFL1 is positive and enables A 1103. When the Phase Counter steps off of PS1 to PS2 or PS6, the output of OR gate 029 goes positive and resets the Common Function FF, thus terminating the function.

The overflow which results from align shift R1 left, or shift R2 left in Multiply or Divide is sensed by OR gate 108. Four timing signals at the input of OR gate 108 define C15 time. TFG1 is a convenient signal which transitions to 0 volts in C15 time, and EDPS2 assures that all the multiplier or dividend has been operated upon before RSL03 can be developed. PS73 and PC12 define PS1 or PS3 or PS5. The output of this gate is used to develop RSL03 in C15 time of PS1 in an align shift R1 left, in C15 time of PS3 in a multiply problem, and in C15 time of PS5 in a divide problem if R2 is being shifted left. MSU3 is applied to OR gate 108 to assure that RSL03 won't be developed in PS5 of divide unless R2 is being shifted left. Thus, as long as the machine is subtracting in PS5 of Divide, the gate is inhibited, but when a carry overflow stops the subtract cycle and shift R2 left begins, MSU3 permits RSL03 to be developed.

Although RSL03 will be developed every PS1, every PS3, and every PS5, it will not interfere with the machine operation in the wrong function.

For example:

Every time the machine goes into PS1, either nothing is done, or MA1L3 (align shift R1 left) is developed. If MA1L3 is developed, the DPS FF must be set, so RSL03 is generated. If the DPS FF is already set when the machine goes into PS1, and MA1L3 is not developed, RSL03 is still generated, but has no effect because the machine does nothing if MA1L3 is not developed.

Every time the machine goes into PS3, either nothing is done (as in the case of a divide problem) and no harm is done by generating RSL03, or R2 is shifted left (as in the case of a multiply problem) and RSL03 will be generated if the DPS FF is set.

Every time the machine goes into PS5 in a multiply problem, either nothing is done, or a count of 1 is added to R2. In either case, it doesn't matter that RSL03 may be developed. Every time the machine goes into PS5 in a divide problem, either RMD is subtracted from R1, and a count of 1 is added to R2, or RMD is added to R1 and R2 is shifted left. If the machine is subtracting in PS5 of Divide, MSU4 inhibits RSL03 to avoid any interaction. If the machine is adding RMD to R1 and shifting R2 left, RSL03 will be developed if the DPS FF is set.

d. MULTIPLY SHIFT R2 LEFT. OR gate 048 generates the signal to shift R2 left in a multiply problem, so naturally one input to OR gate 048 is EMU2. Three other inputs, PC12, PC22, and PC41, define PS3. The two timing signals TFE2 and TFF1 define R2 time, and TCX5 limits the columns involved in the shift R2 left to C2 through C14. The only time the output of OR gate 048 goes negative (logic 0) is in PS3 of Multiply, and only during the R2 times between C2 and C14. The output of OR gate 048 is applied to AND gate 100 and inverter 101 to enable the generation of SAD9 and SDC9.

e. DIVIDE SHIFT R2 LEFT. OR gate 039 is used to generate SAD9 and SDC9 to shift R2 left in Divide. EDV2 is, of course, one input to OR gate 039. Another input is ACOF2. The Carry Overflow flip-flop is set in Divide at the end of the subtract cycle because there is an overdraft. Per the Three Counter machine Divide Flow Chart in Figure 5-3, the next thing to be done is shift R2 left and add RMD to R1. OR gate 039 takes care of shifting

DIVIDE FLOW CHART (3 COUNTER EC-130)

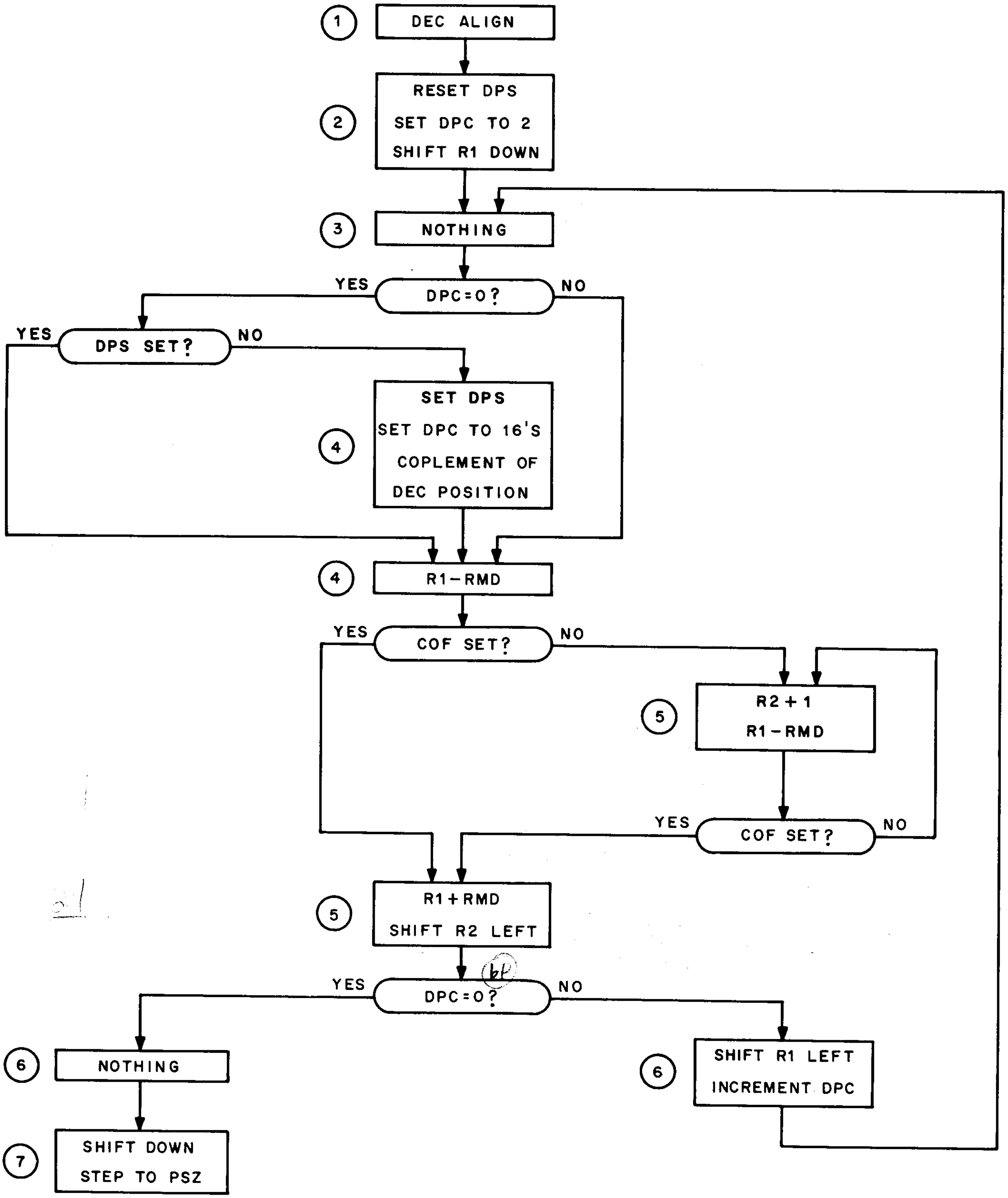

Figure 5-3

R2 left in PS5. TFF1 and TFE2 define R2 time, and TCX5 defines C2 through C15 times.

3. SHIFT UP

Shift up in the Three Counter machine is much the same as in the Four Counter machine. With normal (idle) data flow from the A Counter to the C Counter, to shift up, the data must be shifted from the A Counter to the D Counter, and from the D Counter to the C Counter. Timing is the same in this machine as in the earlier model EC-130. There are three ways to utilize the shift up feature; Repeat, Recall, and the first entry of a digit entry.

a. REPEAT FUNCTION. The Entry Encoder code for Repeat is a binary three. This is reflected in OR gate 090, which is used to generate SAD9; and OR gate 091, which is used to generate SDC9. Both these gates have EEN12 and EEN22 as inputs. (Actually, these two signals alone define a code of three or a code of seven, but since the code seven isn't used, it isn't necessary to have EEN41 on the gates.) The only other input on OR gate 090 is PS64, so SAD9 will be generated every R time in PS6. PS64 is also an input to OR gate 091. But, OR gate 091 also has three other inputs. TC03 assures that SDC9 will not be generated in C0 time (which would create sync pulse problems), TFG1 inhibits SDC9 during RS and RMD times, and TR13 inhibits SDC9 during R1 time. Thus, data is preserved in RS, RMD, and R1 times, and R2, R3, and R4 data is shifted up. This logic is nearly identical to that in the earlier machine.

b. RECALL FUNCTION. Recall is gated by an Entry Encoder code of one. So the two OR gates used to develop SAD9 and SDC9 in recall will have EEN12, EEN21, and EEN41 as inputs. OR gate 089 (used to develop SAD9) has two other inputs; PS64 defines PS6, and TR03 inhibits the development of SAD9 in RMD time. OR gate 088 also has two other inputs. PS64, as in OR gate 089, and TC03, which inhibits SDC9 to preserve the sync pulse in B3 R3 C0 time. This logic is nearly identical to the Recall logic in the Four Counter EC-130.

c. SHIFT UP IN THE DIGIT ENTRY OPERATION. Shift up in a digit entry is gated by OR gate 099. Since the Entry Encoder is not set in a digit entry, no Encoder signals are applied to OR gate 099. Thus, the logic for OR gate 099 is identical to that in the earlier EC-130.

4. SHIFT DOWN

Shift down in this machine is radically different from the method used in the Four Counter machine. A shift down in the normal sense of the word cannot be done because there is no counter which can be bypassed. Shift down in the new EC-130 is a rather more complex idea and a correct concept of timing becomes of paramount importance.

Figure 5-4a shows a portion of the data in a machine as organized on the delay line. Figure 5-4b shows the same data AFTER shifting down R1, R2, R3, and R4. Note that the data that was in R1, R2, R3, and R4 is now 48 μs closer to the sync pulse than before the shift down. In fact, whether a digit is in RS, RMD, R1, R2, R3, or R4 depends solely upon its proximity to the sync pulse.

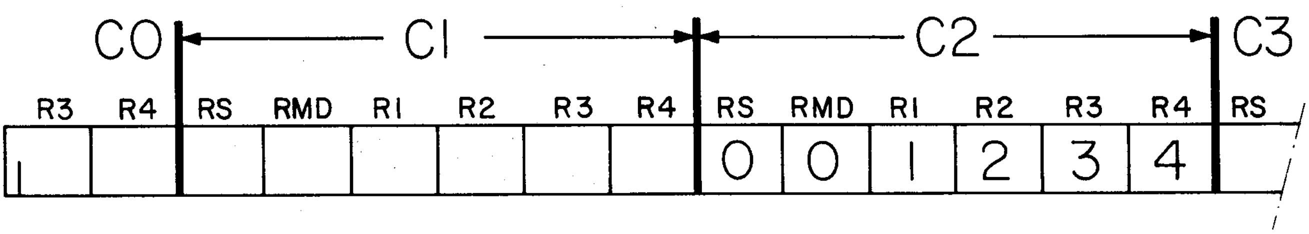

Figure 5-4a

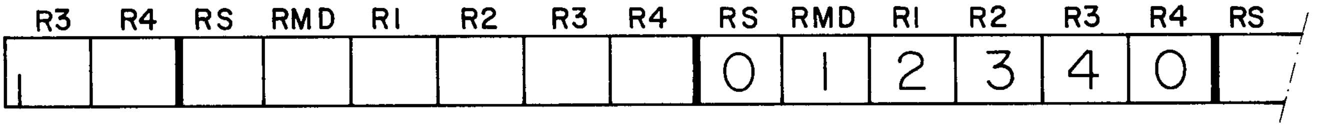

Figure 5-4b

Look at Figure 5-5a. If a single pulse is 480 μs from the sync pulse, it MUST be in R1 C2 time. The act of shifting R1 down merely moves that pulse 48 μs closer to the sync pulse. In Figure 5-5b, that pulse is only 432 μs from the sync pulse. Hence, it MUST be in RMD C2 time. It has been shifted down. Now a general (but important) statement can be made. TO SHIFT DATA DOWN, IT IS NECESSARY ONLY TO MOVE THAT DATA 48 μs CLOSER TO THE SYNC PULSE.

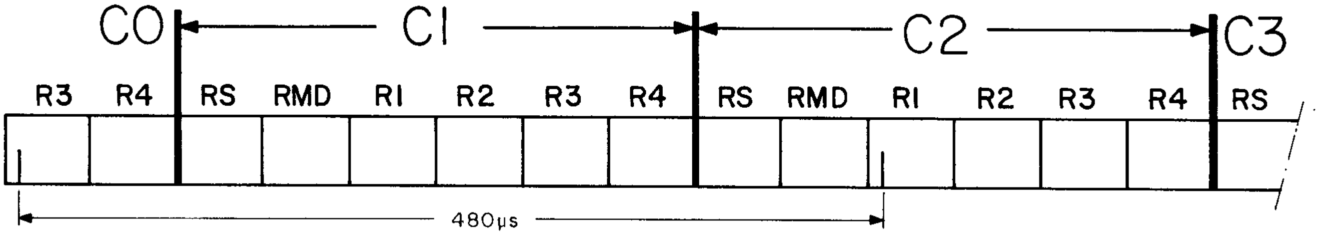

Figure 5-5a

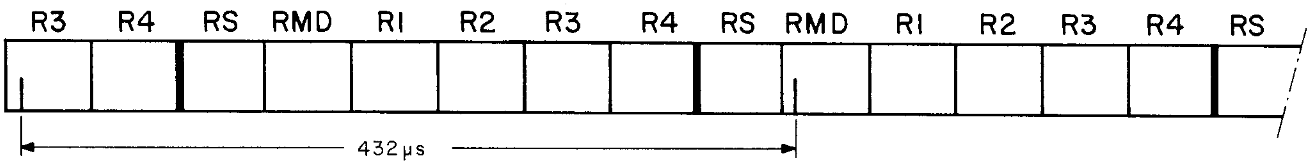

Figure 5-5b

Would the result be the same if the sync pulse were moved closer to the data? At first glance one would say, no! But, look closely at Figure 5-6a which shows the sync pulse in B3 R3 C0, a pulse in B3 R1 C2 (480 μs from the sync pulse), and a pulse in B3 R2 C2 (528 μs from the sync pulse). Now suppose the sync pulse is shifted up to B3 R4 C0, as drawn in Figure 5-6b. This time the sync pulse is moved 48 μs closer to the data instead of vice versa. It appears that there is no change in the position of the data, but now the first pulse (in B3 R1 C2) is only 432 μs and the second is only 480 μs from the sync pulse. When these three pulses count back onto the delay line

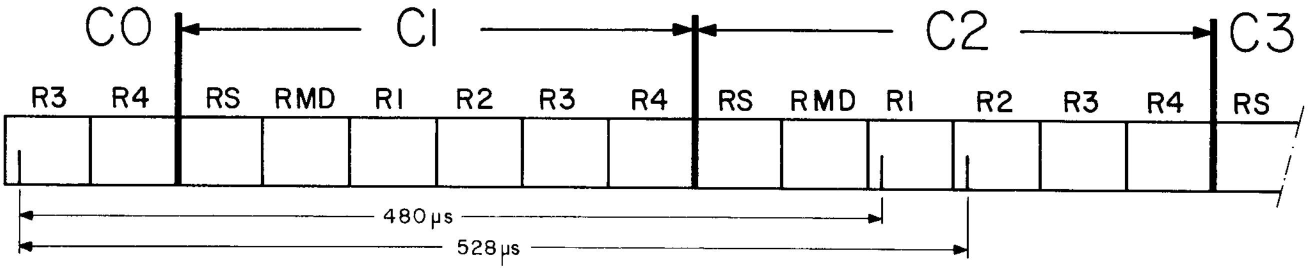

Figure 5-6a

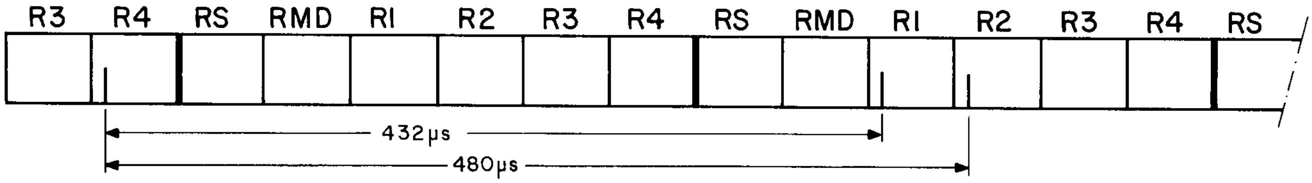

Figure 5-6b

they maintain this time relationship. When the sync pulse counts back off the delay line it is re-established in B3 R3 C0 (Figure 5-6c) time. So the nearest pulse, only 432 µs later, MUST be in RMD C2 time, and the second, 480 µs from the sync pulse, MUST be in R1 C2 time. Clearly, shifting up the sync pulse has the same effect as shifting down data.

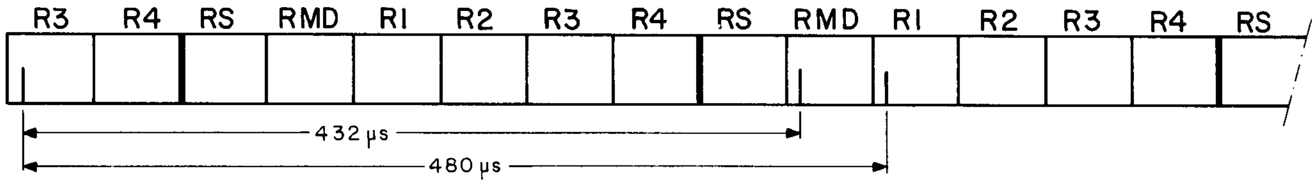

Figure 5-6c

The problem now is that shifting up the sync pulse shifts down ALL data including RS. Fortunately, it is a simple matter to correct this. If RS is shifted up to RMD in the same line pass that the sync pulse is shifted up, then in the next line pass when all data is resynchronized 48 µs early, the original RS data will still be in RS time. For example, suppose there is data in C2 as shown in Figure 5-7a, and R1, R2, R3, and R4 are to be shifted down in a Clear Entry function. Shift down in Clear Entry is done in PS6, so in PS6 when the sync pulse counts off the delay line, it synchronizes the timing chain, thus establishing itself in B3 R3 C0 time, and establishing All data in their proper times. Then the sync pulse is shifted up (delayed 48 µs) into R4 C0 time. Since the timing chain is already running, this has no effect on the data as it counts off the delay line. As this data comes off the delay line, all RS data is shifted up (delayed 48 µs) into RMD time (see Figure 5-7b). When the sync pulse counts off the delay in the next line pass (PS7), it resynchronizes the timing chain so that all data is shifted down, and the RS data that was shifted up into RMD is once again in RS time R1, R2, R3, and R4 data are shifted down as shown in Figure 5-7c.

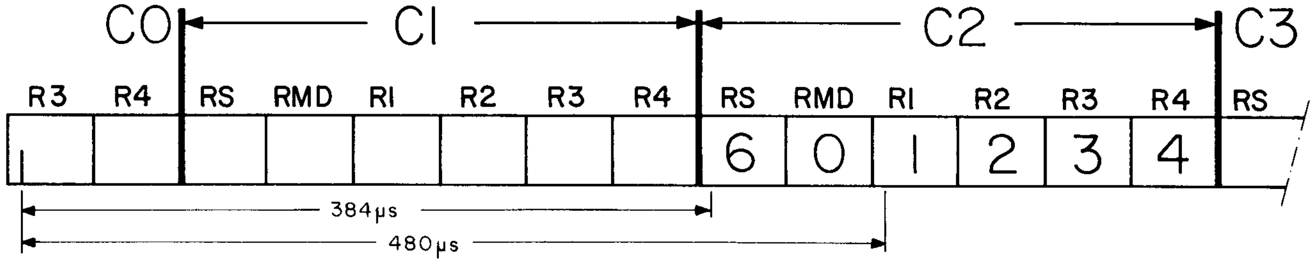

Figure 5-7a

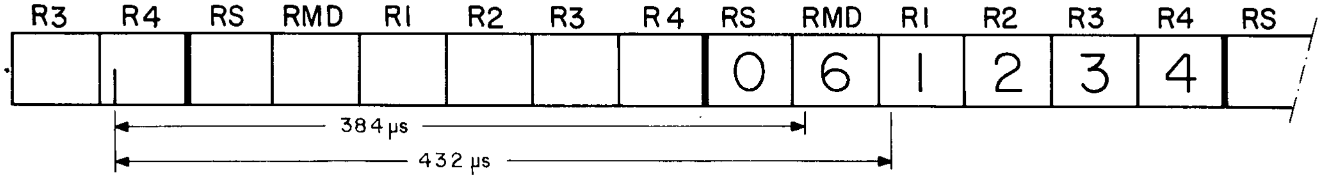

Figure 5-7b

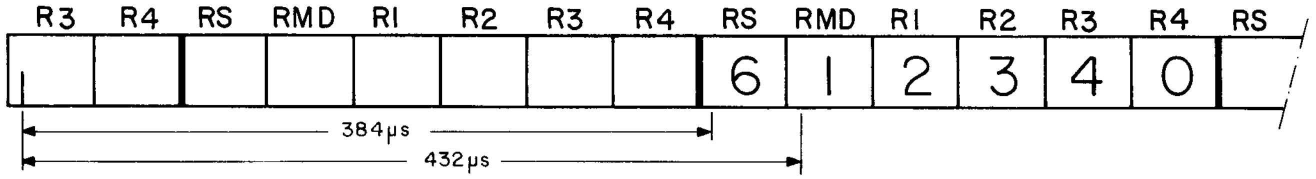

Figure 5-7c

a. SHIFT DOWN R1, R2, R3, R4 IN CLEAR ENTRY, ADD, SUBTRACT, MULTIPLY AND DIVIDE. This, then, is the basic theory of shift down. The operation just described occurs in PS6 of Clear Entry. But the same thing happens in PS6 of the Add, Subtract, and Store functions as well as in the Clear Entry function. The two OR gates that are used to shift up the sync pulse and RS are OR gate 310 and OR gate 304. OR gate 310 is used to generate SAD9 and SDC9 in C0 time to shift up the sync pulse in the Clear Entry, Add, Subtract, and Store functions. PS64 is one input to OR gate 310 and enables the sync pulse to be shifted up only in PS6. EEN42 is another input because the only time EEN4 FF is set is in any one of the above functions. The third input to OR gate 310 is TC04. Thus, OR gate 310 enables SAD9 and SDC9 to be developed in R3 C0 and R4 C0. OR gate 304 enables SAD9 and SDC9 to be developed in RS and RMD of all C times to restore RS to its original position with respect to the sync pulse. There are three inputs to OR gate 304 EEN42 gates for Add, Subtract, Store, or Clear Entry, and PS64 gates for PS6. TFG2 inhibits the OR gate during R1, R2, R3, and R4 times. So OR gate 304 enables SAD9 and SDC9 during RS and RMD times. This will put RS data in RMD time and leave RMD data in the D Counter. If this is left in the D Counter, it will be placed in the next RS time when the next SAD9 and SDC9 are developed. Hence, CRD9 must be developed to clear RMD out of the D Counter. OR gate 305 will enable CRD9 when its output is logic 0 (negative). Two inputs to O-305 are EEN42 and PS64, the same as on O-304. TR14 is the third input to O-305. This means that when O-304 is gating SAD9 and SDC9 to shift RS up, O-305 enables CRD9 to reset the RMD data out of the D Counter in the following R1 time.

The net effect of the operation of OR gates 310, 304, and 305 is that R1, R2, R3, and R4 are shifted down, and RS remains in RS in the Add, Subtract, Store, and Clear Entry functions.

b. SHIFT DOWN R1 IN MULTIPLY AND DIVIDE. To shift down R1, R2, R3, and R4 in PS7 of Multiply or Divide, OR gates 308, 302, and 303 are operated. OR gate 308 enables the sync pulse to be shifted up only in PS7 of Multiply or Divide. OR gate 302 is responsible for enabling SAD9 and SDC9 in RS and RMD of all column times to shift up RS in PS7 of Multiply or Divide. (TFG2 is negative during RS and RMD times). As before, the RMD data must be cleared out of the D Counter each column time, and OR gate 303 enabled CRD9 to be generated at the end of each R1 time in PS7 of Multiply or Divide.

Doesn't matter when as long as it's before next C time.

To shift down R1 and clear R1 to zero in PS2 of Multiply or Divide, it is necessary to shift up the sync pulse, then shift up RS, R2, R3, and R4 causing that data to remain in synchronization to keep it where it was. This puts R1 in RMD. Two OR gates are used to accomplish this. OR gate 306 enables SAD9 and SDC9 in each R time of PS2 except R1 time. (Remember that the only time the machine steps to PS2 is in Multiply or Divide, and we ALWAYS want to shift R1 down to RMD in PS2.) This means that all R times except R1 time are shifted up with the sync pulse. This puts all R times except R1 in their original positions with respect to the sync pulse. R1 is 48 μs closer to the sync pulse, which is effectively a shift down of R1, however, the method described has a drawback. SAD9 and SDC9 are generated for each R time except R1. At the end of RS time, SAD9 and SDC9 are generated, and RS data goes to the D Counter. Whatever was in the D Counter goes to RS time in the C Counter. At the end of RMD time SAD9 and SDC9 are again generated; RMD data goes to the D Counter, and RS data goes to RMD time in the C Counter. SAD9 and SDC9 are inhibited in R1 time so the RMD data ~~stays in the~~ D Counter. At the end of R2 time SAD9 and SDC9 are again generated; R2 data is shifted into the D Counter, and the contents of the D Counter (RMD data) is shifted into R2 time. This means that in the next line pass when the results of shifting up the sync pulse are seen, R1 will have been shifted down to RMD as expected, but RMD will have been shifted up into R1. This is grossly wrong! R1 must be cleared out so that the multiplier or dividend in R2 can be shifted into R1, digit by digit. If RMD is shifted into R1, it will appear to the machine that the RMD data is the most significant part of the multiplier or dividend. Clearly, RMD must not be allowed to reach R1 time. The easiest way to stop it is to reset the D Counter to zero when RMD data is present in the D Counter. Then when SAD9 and SDC9 are generated at the end of R2 time, zeros will be shifted into R2. The RMD data is shifted into the D Counter at B15 RMD time and the next SDC9 will occur at B15 R2 time. Between these two times, the D Counter must be reset to zero. The obvious time to do this is B15 R1 time. OR gate 050 enables CRD9 in each R1 time in PS2. The three Phase Counter signals define PS2, and TR14 defines R1 time. No other signals are necessary because the only time the machine is in PS2 is in Multiply or Divide.

OK Reset D after R1 at end via ~~O-~~ O-050

c. STORE FUNCTION. Shift down in Store is a little different because R1 data must be advanced twice. This means that the sync pulse must be shifted up twice in addition to shifting up other R times to keep them in the right position with respect to the sync pulse. OR gates 310, 304, and 312 are used to accomplish this.

You are already familiar with the operation of OR gates 310 and 304. They are used to shift down they maintain this time relationship. When the sync pulse counts back off the delay line it is re-established in B3 R3 C0 (Figure 5-6c) time. So the nearest pulse, only 432 μs later, MUST be in RMD C2 time, and the second, 480 μs from the sync pulse, MUST be in R1 C2 time. Clearly, shifting up the sync pulse has the same effect as shifting down data.

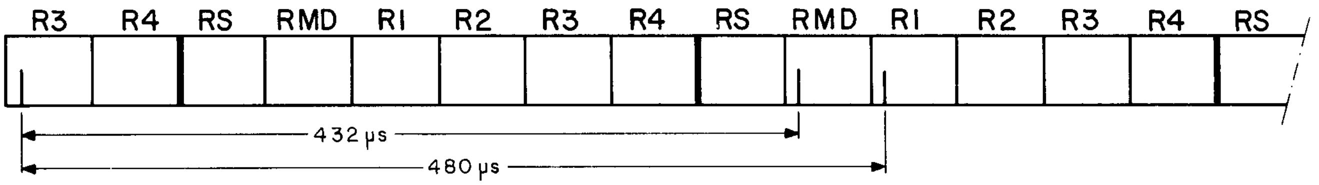

Figure 5-6c

The problem now is that shifting up the sync pulse shifts down ALL data including RS. Fortunately, it is a simple matter to correct this. If RS is shifted up to RMD in the same line pass that the sync pulse is shifted up, then in the next line pass when all data is resynchronized 48 μs early, the original RS data will still be in RS time. For example, suppose there is data in C2 as shown in Figure 5-7a, and R1, R2, R3, and R4 are to be shifted down in a Clear Entry function. Shift down in Clear Entry is done in PS6, so in PS6 when the sync pulse counts off the delay line, it synchronizes the timing chain, thus establishing itself in B3 R3 C0 time, and establishing All data in their proper times. Then the sync pulse is shifted up (delayed 48 μs) into R4 C0 time. Since the timing chain is already running, this has no effect on the data as it counts off the delay line. As this data comes off the delay line, all RS data is shifted up (delayed 48 μs) into RMD time (see Figure 5-7b). When the sync pulse counts off the delay in the next line pass (PS7), it resynchronizes the timing chain so that all data is shifted down, and the RS data that was shifted up into RMD is once again in RS time R1, R2, R3, and R4 data are shifted down as shown in Figure 5-7c.

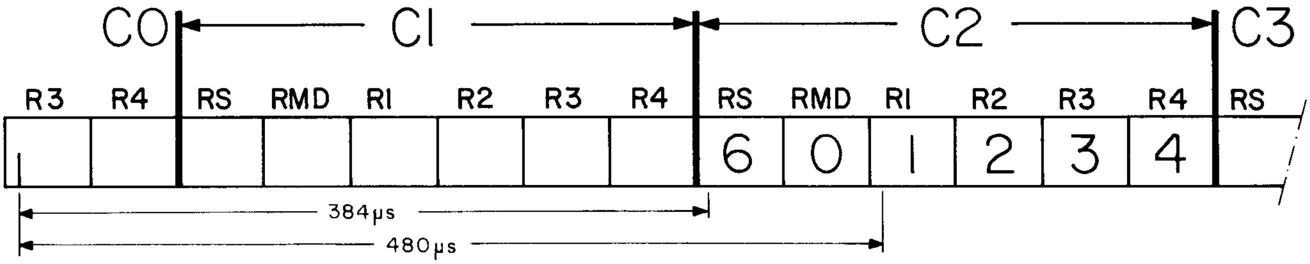

Figure 5-7a

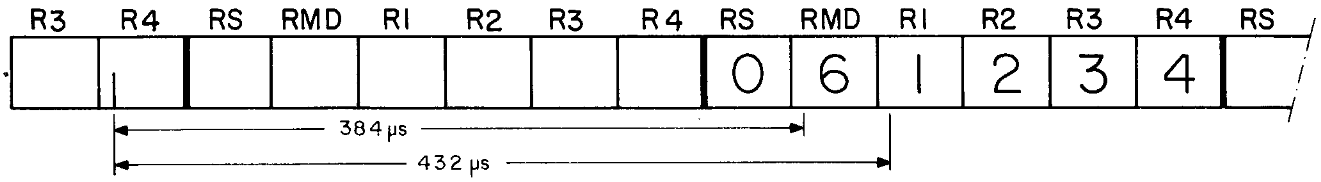

Figure 5-7b

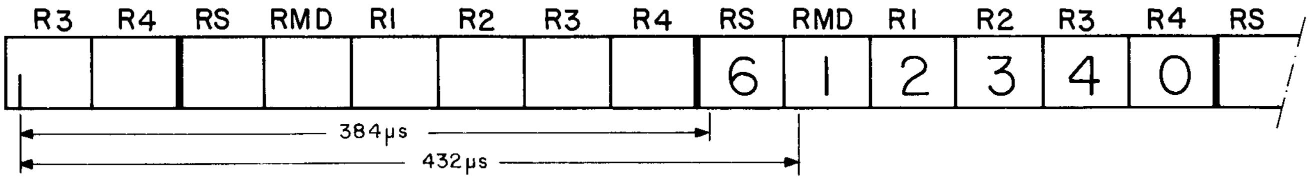

Figure 5-7c

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The net effect of the operation of OR gates 310, 304, and 305 is that R1, R2, R3, and R4 are shifted down, and RS remains in RS in the Add, Subtract, Store, and Clear Entry functions.

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Doesn't matter when as long as it's before next C time.

To shift down R1 and clear R1 to zero in PS2 of Multiply or Divide, it is necessary to shift up the sync pulse, then shift up RS, R2, R3, and R4 causing that data to remain in synchronization to keep it where it was. This puts R1 in RMD. Two OR gates are used to accomplish this. OR gate 306 enables SAD9 and SDC9 in each R time of PS2 except R1 time. (Remember that the only time the machine steps to PS2 is in Multiply or Divide, and we ALWAYS want to shift R1 down to RMD in PS2.) This means that all R times except R1 time are shifted up with the sync pulse. This puts all R times except R1 in their original positions with respect to the sync pulse. R1 is 48 µs closer to the sync pulse, which is effectively a shift down of R1, however, the method described has a drawback. SAD9 and SDC9 are generated for each R time except R1. At the end of RS time, SAD9 and SDC9 are generated, and RS data goes to the D Counter. Whatever was in the D Counter goes to RS time in the C Counter. At the end of RMD time SAD9 and SDC9 are again generated; RMD data goes to the D Counter, and RS data goes to RMD time in the C Counter. SAD9 and SDC9 are inhibited in R1 time so the RMD data ~~stays in the~~ D Counter. At the end of R2 time SAD9 and SDC9 are again generated; R2 data is shifted into the D Counter, and the contents of the D Counter (RMD data) is shifted into R2 time. This means that in the next line pass when the results of shifting up the sync pulse are seen, R1 will have been shifted down to RMD as expected, but RMD will have been shifted up into R1. This is grossly wrong! R1 must be cleared out so that the multiplier or dividend in R2 can be shifted into R1, digit by digit. If RMD is shifted into R1, it will appear to the machine that the RMD data is the most significant part of the multiplier or dividend. Clearly, RMD must not be allowed to reach R1 time. The easiest way to stop it is to reset the D Counter to zero when RMD data is present in the D Counter. Then when SAD9 and SDC9 are generated at the end of R2 time, zeros will be shifted into R2. The RMD data is shifted into the D Counter at B15 RMD time and the next SDC9 will occur at B15 R2 time. Between these two times, the D Counter must be reset to zero. The obvious time to do this is B15 R1 time. OR gate 050 enables CRD9 in each R1 time in PS2. The three Phase Counter signals define PS2, and TR14 defines R1 time. No other signals are necessary because the only time the machine is in PS2 is in Multiply or Divide.

OK at end
Reset D at R1 via O-050

c. STORE FUNCTION. Shift down in Store is a little different because R1 data must be advanced twice. This means that the sync pulse must be shifted up twice in addition to shifting up other R times to keep them in the right position with respect to the sync pulse. OR gates 310, 304, and 312 are used to accomplish this.

You are already familiar with the operation of OR gates 310 and 304. They are used to shift down

R1, R2, R3, and R4 in Add, Subtract, Clear Entry, and Store. These two gates put R1 data in RMD time, R2 data in R1 time, R3 data in R2 time, and R4 data in R3 time. R4 is left empty. This takes one line pass and is done in PS6. The only thing remaining to be done is to put the data now in RMD into RS, but it is equally important NOT to further shift down all the other R times. Since shifting the sync pulse up is the same as shifting ALL data down, in addition to shifting up the sync pulse, we must shift up all R times except RMD. OR gate 312 performs this operation in PS7 of Store. EEN42 and EEN22 define the Store function, PS74 gates for PS7, and TR03 inhibits the output during RMD time. Hence, OR gate 312 enables SAD9 and SDC9 for the sync pulse, RS, R1, R2, R3, and R4.

In conclusion, shift down is not difficult to understand as long as the student thoroughly understands basic data organization.

(TECHNICIAN)

F. ADD FUNCTION

To begin the Add function the Entry Encoder must first be set to a binary code of five. This is the code for both the Add and Subtract functions and corresponds to setting the Add or Subtract FF in the Four Counter machine.

1. ENTRY ENCODER LOGIC

When the Add switch is closed, 0 volts is applied to OR gates 322 and 324. This 0 volts enables AC AND gates 1663 and 1681 to set EEN4 FF and EEN1 FF, respectively. EKBD3 is the AC input to all the gates which set the Entry Encoder flip-flops, so after about 6 ms the Entry Encoder is set to a binary code of five.

When the Phase Counter steps to PS1, OR gate 053 will develop MAIL3 until R1 is decimal aligned, then the Phase Counter will jump to PS6.

2. SIGN CONTROL LOGIC

In PS6, two things are done:

(a) The Sign Control FF checks the signs of R1 and R2 to determine if the ultimate operation will be an addition or subtraction. The Sign Control FF is normally clamped in the set condition during machine idle by ERF3 applied to ASC1 as an override set. If the flip-flop is still set at the beginning of PS7, the machine will add; if it is in the reset condition at the beginning of PS7, the machine will subtract. OR gate 007 samples the signs of R1 and R2, and to do this it must have several inputs. EEN12 and EEN42 gate for an Add or Subtract function. TC14 and PS64 limit the sampling to C1 time of PS6. TFF1 further limits the sampling to R1 and R2 times, and XRDL4 provides the actual sign information from the delay line. If all these conditions are met, and there is a minus sign in R1 or in R2, the output of OR gate 007 will go negative (logic 0) for about 1 us. This negative transition is inverted by I-008 and will reset the Sign Control FF. If the Sign Control FF remains reset, the machine will subtract. But if there are minus signs in both R1 and R2, there will be two transitions at the output of OR gate 007; the first will reset the flip-flop, and the second will set it again, and the machine will add. If both the signs of R1 and R2 are positive, there will be no transitions to reset the flip-flop and the machine will add. It will be assumed that the Sign Control FF is in the set condition at the end of PS6.

(b) The second thing which occurs in PS6 is the shift down of R1, R2, R3, and R4. Recall that this is accomplished by shifting the sync pulse up, which is the same as shifting everything down. Then RS is shifted up to put the RS data back in RS time. Since both are done in the same line pass, it appears (and indeed is true) that the sync pulse is shifted up to B3 R4 C0, and that each RS data is shifted up into RMD time. But when the sync pulse counts off the delay line in PS7, it is re-established in B3 R3 C0 time (48 μs earlier than it was in PS6 after the shift up), and thus ALL data is re-established 48 μs earlier in PS7. This amounts to a shift down of R1, R2, R3, and R4. OR gate 310 enables SAD 9 and SDC9 when its output is negative. Its output will be negative in C0 time of PS6 in Add or Subtract. OR gate 304 enables SAD9 and SDC9 in each RS and RMD time of PS6 in Add or Subtract. (Additional shift down information can be obtained under Topic E4).

3. DEVELOPMENT OF MAD4

In PS7 the actual addition is done. Once again assuming that the Sign Control FF was in the set condition at the end of PS6, ASC2 is negative and ASC1 is positive. Because ASC1 is positive at the input of OR gate 023, MSU4 cannot be generated, but ASC2 is negative and is an input to OR gate 021. When the output of OR gate 021 goes negative MAD4 will be generated. The other three inputs to OR gate 021 define PS7 and the Add or Subtract functions. In either an Add or Subtract function, the Entry Encoder is set to a binary code of five, hence the use of EEN12 and EEN42. So the only time the output of OR gate 021 will be negative is in PS7 of an Add or Subtract function when the Sign Control FF is set. ASC2 assures that the function is Add instead of Subtract. When the output of O-021 goes negative, it causes MAD4 to be developed by I-020.

4. OVERFLOW

If the addition yields an overflow, the overflow is sensed by the setting of the Carry Overflow FF. ACOF1 is the AC input to AC AND gate 1221 on the Overflow FF. The DC input to 1221 is MA1S3. Anytime the Carry Overflow FF sets in an Add function, the Overflow FF will be set by AC AND gate 1221. (Note: OR gate 311, which generates MA1S3 in a Divide, cannot cause MA1S3 to be generated before the Carry Overflow FF is set (ACOF2 negative). This means that ACOF1 has already transitioned positive BEFORE MA1S3 can go positive. Hence, in a Divide, the trigger occurs before the DC enable, and AC AND gate 1221 cannot set the Overflow FF.)

G. SUBTRACT FUNCTION

The basic Subtract function is the same as in the earlier EC-130, however, there are some changes, mainly caused by using the Entry Encoder.

1. ENTRY ENCODER LOGIC

The Entry Encoder is set exactly the same way as in Add. When the Subtract switch is closed, the diode connecting it to the Add switch becomes forward biased to permit EEN4 FF and EEN1 FF to be set by EKBD3. The Subtract switch output is also used as a DC enable to AC AND gate 1143 (Sign Control FF). When EKBD3 transitions positive, A-1143 will reset the Sign Control FF. If the Sign Control FF stays reset, the machine will subtract. Whether the Sign Control FF stays reset will depend upon the result of checking the signs of R1 and R2 in PS6.

When the Phase Counter steps to PS1, an align shift R1 left will be generated if necessary by OR gate 053. After the alignment is completed, the Phase Counter jumps to PS6.

2. SIGN CONTROL AND SHIFT DOWN LOGIC

In PS6 two things will be accomplished. The Sign Control FF checks the signs of R1 and R2 to determine whether the ultimate operation will be an addition or a subtraction. Recall that the Subtract switch reset the Sign Control FF at the beginning of the function. If the Sign Control FF is in the reset condition at the end of PS6, a subtract operation will be performed; if it is in the set condition at the end of PS6, the machine will add.

There are six inputs to OR gate 007 to gate for the signs of R1 and R2. EEN12 and EEN42 define the Add or Subtract functions. PS64 limits the sampling to PS6 time and TC14 further limits the sampling to column one. TFF1 is negative only during R1 and R2, so the only time the output of O-007 can possible go negative (logic 0) is during R1 or R2 of C1 time in PS6 or an Add or Subtract function. If there is a pulse in R1 C1 time it means that the sign of R1 is negative. If the sign of R1 is negative, XRDL4 will transition negative in R1 C1 time and the output of O-007 will go negative. This is inverted by I-008 whose output is applied to the T input of the Sign Control FF. Since the flip-flop is already reset, the output of the inverter will set the flip-flop. If the Sign Control FF stays set, the machine will add. If, however, there is a minus sign in R2 as well as in R1, the output of I-008 will transition positive twice, resetting the flip-flop with the second pulse, and the machine will subtract.

R1, R2, R3, and R4 are shifted down. The machine does this by shifting up the sync pulse and RS. The sync pulse is shifted up by gating to enable SAD9 and SDC9 during each R time of C0 time. OR gate 310 accomplishes this. EEN42 gates for the Add, Subtract, Clear Entry, or Store functions. TC04 enables the OR gate in all R times of C0 time, and PSG4 limits the operation of the gate to PS6 time. So the output of the gate is negative in R3 or R4 of C0 time in PS6 of Subtract. When the output of O-310 is negative, SAD9 and SDC9 are enabled and this results in the shift up of the sync pulse.

OR gate 304 is used to enable SAD9 and SDC9 in RS and RMD to shift up RS. EEN42 and PS64 gate for PS6 of an Add, Subtract, Clear Entry, or Store function. TFG2 is negative during RS and RMD times. So the output of O-304 will be negative to enable SAD9 and SDC9 in each RS and RMD times. At the end of RS time RS is shifted to the D Counter. At the end of RMD time, RMD is shifted to the D Counter, and RS is shifted into RMD time at the C Counter. This leaves RMD in the D Counter. If the RMD data is in the D Counter at the end of the next RS time, this data will be shifted into RS time. To avoid this, the D Counter is reset each R1 time. This is done by OR gate 305. EEN42 gates for Add, Subtract, Clear Entry, or Store. PS64 and TR14 gate for each R1 time in PS6, and the output of O-305 will go negative for 48 µs at this time. Any negative input to AND gate 309 will cause CRD9 to be developed by elements 144 and 145.

So, OR gates 310, 304, and 305 are operated to shift down R1, R2, R3, and R4 in PS6 of a Subtract problem. (For additional shift down information, see Topic E4.)

3. THE DEVELOPMENT OF MSU4

The actual subtract operation is done in PS7. Again it must be assumed that the Sign Control FF is in the reset condition. If it is, then ASC2 is positive to inhibit the generation of MAD4. ASC1 is negative. This signal is one of three inputs to OR gate 023 and enables O-023. PS74 gates for PS7, and ACOF1 must always be negative at the beginning of PS7. (The reason ACOF1 is there is because in this machine if it is necessary to complement R1, the complement is done in PS7 instead of in PSZ as in the Four Counter EC-130. Since MSU3 must be inhibited if the complement is being taken, ACOF1 is used to inhibit gate 023 at this time.) Thus, the output of OR gate 023 goes negative for one line pass. This makes the output of AND gate 046 negative and the output of I-070 positive. This signal is MSU3. MSU3 is the input of I-073 and MSU4 is an input to OR gate 071. The output of this gate is inverted and used to inhibit CRA9, and to enable C1D9. MSU4 is also applied to O-146 with TCX5, TRO4, and TB154 to develop SDA9 each RMD time to place the complement of RMD into the A Counter for addition with R1. The rest of the basic subtract logic is identical to that of the earlier EC-130 and will not be covered.

MSU3 is positive at the end of subtract and inhibits the Phase Counter from being stepped to PSZ. But, PS73 and HOME1 are anded at AND gate 1104 to reset the Common Function FF. When ECF1 goes negative ECFD4 goes positive and clamps the Phase Counter to PSZ with the override resets. ECFD4 also generates ERF3 to reset the Entry Encoder FF's and set the Sign Control FF.

4. COMPLEMENT

If the Carry Overflow FF is set at the end of the subtract operation, it is indicative of the necessity to complement R1 and change the sign of R1. Then ACOF1 will be positive at the input to OR gate 016 (which develops ECFD4) and inhibits the generation of ECFD4. ECFD4 stays negative even though the Common Function FF is reset, and thus the Phase Counter is not clamped to PSZ. It stays at PS7, and R1 will be complemented in PS7. There is also one other effect of ECFD4 staying negative. The Sign Control FF stays reset. Normally, if the Sign Control FF is reset in PS7, OR gate 023 will generate MSU3. However, ACOF1 is now positive and inhibits the gate. So the purpose of having ACOF1 as an input to OR gate 023 is to inhibit the subtract operation during the complementing of R1. Of course, after the complement of R1 is completed, HOME1 resets the Carry Overflow FF and ECFD4 (elements 016 and 017) goes positive. This results in clamping the Phase Counter to PSZ, and setting the Sign Control FF with the override set input.

H. CHANGE SIGN OF R1

The logic used in changing the sign of R1 in this machine agrees with the logic used in the Four Counter machine. The idea is to add a count of one to R1 C1 time. If R1 C1 contains a zero (no minus sign) then the addition of a count of one puts a one (minus sign) in R1 C1. If there is already a count of one (minus sign) in R1, the addition of a count of one puts a two in R1. This count of two is promptly cleared to zero (no minus sign). The count of one is added to R1 C1 time by generating ASA13 to set the A1 FF at the end of RMD C1 time. There are five ways of generating ASA13, and two of them are used to change the sign of R1. These two are described as follows:

1. SUBTRACT FUNCTION

OR gate 081 (located on the logic print between the Phase Counter and the Carry FF) will cause I-111 to generate ASA13 when the output of O-081 goes negative. The first condition is that the Sign Control FF must be reset (which defines a subtract function). This is gated by ASC1. The second condition is that the Carry Overflow FF must be set (showing the necessity of complementing R1 and changing the sign of R1). This is gated by ACOF2. TRO4 and TC14 define RMD C1 time and the output of O-081 will go negative for 48 µs and cause ASA13 to go positive for 48us. When ASA13 is positive, A1 FF is enabled to be set by CRA9.

Then the contents of R1 C1 can count in on top of the count of one already in the A Counter. If there was nothing in R1 C1 then the new count will be a one (minus sign). Thus, nothing else needs to be done. But if the sign of R1 was already minus with a count of one in R1 C1, then the addition of a count of one will put a two in R1 C1. This is an invalid code for sign information and this "two" must be cleared out to zero (the valid code to show that the sign of R1 is positive). AC AND gate 1297 at the input to the A1 FF detects any invalid code in C1 time. If the A2 FF sets any time in C1 time, it is indicative of an invalid code for the sign information. TC13 is the DC input to A-1297 and limits the operation of the gate to the time that sign information is counting into the A Counter. CA21 is the trigger input to A-1297. If the A2 FF sets, CA21 goes positive and resets the A1 FF. (Recall that in the Four Counter machine this was done in the B Counter, and both the B1 FF and the B2 FF were reset.) In this machine, however, the A2 FF stays set. At the end of R1 C1 time this illegal counter code is shifted to the C Counter. Because the C1 FF and the C5 FF are reset, CCZ3 is positive indicating that the C Counter is zero, and C1C9 is inhibited. Hence, the C2 FF stays set. Complications are avoided by leaving the reset gates on the C2 FF, so that the C2 FF is reset by the succeeding A to C shift of D to C shift if the incoming data is not supposed to have the C2 FF set. If the incoming data is supposed to have the C2 FF set there is no problem. It is already set.

2. CHANGE SIGN FUNCTION

The other way ASA13 can be used to change the sign of R1 is by operating OR gate 077. When the output of OR gate 077 goes negative, the sign of R1 will be changed as described in Topic H1. OR gate 077 is used in conjunction with the Change Sign Key. When the Change Sign switch is closed, EEN2 FF is enabled to be set by EKBD3. EEN1 FF and EEN4 FF remain reset. In PS1 the data in R1 is decimal aligned if necessary (see Topic E3 for align shift R1 left information). After the decimal alignment, the Phase Counter jumps to PS6. In PS6 the actual change sign operation takes place. OR gate 077 is gated by EEN11, EEN22, and EEN41 for the Change Sign function only. PS64 limits the operation of the gate to PS6. TR14 and TC14 define R1 C1 time so the output of O-077 will go negative only during T1 C1 time in PS6 of a Change Sign function. When the output of this gate goes negative, the sign of R1 is changed as described in Topic G2. In PS7, nothing is done and the machine terminates the function at the end of PS7.

3. MULTIPLY OR DIVIDE FUNCTION

Changing the sign of R1 in Multiply and Divide is explained in the description of those functions.

J. MULTIPLY FUNCTION

The Multiply logic is essentially the same in this machine as in the earlier EC-130. The changes are minor and are a product of a more efficient use of parts.

1. MULTIPLY FLOW CHART

The Multiply Flow Chart is shown in Figure 5-8. (See Foldout Page 23 .) This Flow Chart should be compared with the Multiply Flow Chart of the Four Counter EC-130. While there are differences, the operation is done in the same order in both machines. Because of the similarity of operation, learning the Multiply function of the Three Counter machine will present no special problems. The Multiply function is explained by Phase Counter step in the following explanation.

2. DECIMAL ALIGN (PS1)

As in the Four Counter machine, PS1 is devoted exclusively to the decimal alignment of the contents of R1. MAIL3 is developed by elements 053 and 054, and MAIL3 in turn causes MIL4 to be developed. MIL4 is one of four inputs to OR gate 097. TCX5 and TR14 gate for all R1 times from C2 through C14 (C15 in Divide). Since RSL03 is developed only in C15 time, and O-097 is inhibited in C15 time in a Multiply function, it has no logic function as an input to O-097 in Multiply. So when the output of O-097 goes low, it causes SAD9 and SDC9 to be generated every R1 time in columns C2 through C14 to shift R1 left.

3. CHANGE SIGN OF R1 (PS2)

In PS2 of a Multiply problem the same things must be done that are done in PS2 in the earlier EC-130. First, the sign of R1 is added to the sign of R2. OR gate 051 and inverter 052 are used to generate AIRX3 which inhibits the generation of CRA9 when AIRX3 is logic 1. (The logic used to develop AIRX3 is identical to the logic in the Four Counter machine and will not be further discussed). AIRX3 also is used to reset the DPS FF and to set a count of 4 into the Decimal Point Counter.

4. SHIFT DOWN R1 TO RMD

The other thing done in PS2 is the shift down of R1. To shift down R1, it is necessary to shift up the sync pulse, and all data except R1. In addition, because it is necessary to clear R1 out to zero, CRD9 must be generated each R1 time to reset the RMD data out of the D Counter. If this is not done, RMD data will end up in R1 time. OR gate 306 causes SAD9 and SDC9 to be generated each R time except R1 time in PS2 including R3 C0 time for the sync pulse. This results in the sync pulse and all data except R1 data being shifted down. OR gate 307 is used to clear the RMD data out of the D Counter. The output of O-307 goes negative each R1 time in PS2 and causes CRD9 to be generated each time it goes negative. Developing CRD9 in R1 time clears out the RMD data before it can be shifted into R2 time. (For more detailed information on Shifting Down R1, see Topic E4.)

An overflow in the Multiply function is detected in this machine in the same way as in the Four Counter machine. Once the Decimal Point Counter has been counted to zero, and the DPS FF has been set, RSL03 is developed each PS3 time. If there is any data remaining in the D Counter when RSL03 is developed, CRD9 will clear the D Counter to zero, and the Overflow flip-flop will be set. The function will not be interrupted so the decimal alignment is allowed to continue to its ultimate conclusion. RSL03 is developed by OR gate 108 and Inverter 109. The four timing signal inputs to O-108 limit the operation to R1, R2, R3, and R4 of C15 time. EDPS2 assures that the DPS FF is set, and MSU3 inhibits the gate during a Subtract function. PS73 and PS12 gate for PS1, PS3, or PS5. When the output of I-109 goes positive, the output of I-143 goes negative to enable CRD9 to be developed. When the output of I-109 goes positive and there is data in the D Counter, AC AND gate 1222 causes the Overflow flip-flop to be set. (For additional Shift Left Overflow information, see Topic E2.)

5. SHIFT R2 LEFT (PS3)

In PS3 of Multiply, the same thing is done in this machine that is done in the Four Counter machine. R2 must be shifted left. Shift R2 left is controlled by OR gate 048 which causes SAD9 and SDC9 to be developed when its output goes negative. PC41, PC22, and PC12 at the input of O-048 define PS3. EMU2 limits the operation of the gate to the Multiply function, and TCX5 inhibits the gate in C0, C1, and C15 times. TFE2 and TFF1 define R2 time, so the output will go negative each R2 time, C2 through C14 in PS3 of a Multiply function.

6. ADD IN MULTIPLY FUNCTION (PS4)

An overflow in a Multiply is detected in PS3 in the same manner used in the Four Counter machine. If there is a digit other than zero in the D Counter when RSL03 is developed, the D Counter will be reset to zero by CRD9, and the Overflow FF will be set by AC AND gate 1222. (For additional shift left overflow information, see Topic E2c.)

Everything that is done in PS4 and PS5 of Multiply in the Four Counter machine is done in PS4 in the Three Counter machine. The first operation occurs at the beginning of PS4. If the Decimal Point Counter is zero, and the Decimal Point Storage FF is reset, the DPS FF will be set by AC AND gate 1133. The enable input to A-1133 is DSZ3. The AC trigger input comes from OR gate 011. The two inputs to O-011 are EMD4 and PC41. EMD4 and PC41 are both negative in PS3 of Multiply, so the output of O-011 is negative. PC41 goes positive at the beginning of PS4 so the output of O-011 goes positive. This positive transition will set the DPS FF if DSZ3 is also positive. When the DPS FF sets, EDPS1 transitions positive. EDPS1 is used to set the Decimal Point Counter to a count of three plus the decimal position.

The add cycles are also done in PS4. To add in a multiply problem, it is necessary to generate MAD4. When the output of OR gate 041 goes negative, MAIM3 goes positive which causes MAD4 to go negative. To get the output of O-041 negative it is necessary to have all inputs negative. EMU2 is always negative in a multiply problem. PC42 and PC22 define PS4 or PS5 (although it will be seen shortly that the entire add cycle is done in PS4). CDZ3 is negative as long as there is a digit other than zero in the D Counter. When the output of O-041 goes negative, MAD4 is caused to go negative and enables OR gate 074 to develop AIRA3. (For more detailed information on addition see Topic F.)

7. INCREMENT D COUNTER

At the end of each addition in C15 time OR gate 134 causes the D Counter to be incremented. TFH2, TFJ2, TFK2, and TFL2 define C15 time. TR14 defines R1 time, and MAD4 and EMU2 define an addition in a Multiply function. Hence, OR gate 134 will cause the D Counter to be incremented once for each add cycle. The logic for O-134 is the same as in the earlier machine.

8. CARRY OVERFLOW AND CARRY

If there is a carry overflow, or a carry overflow and a carry, R2 is incremented by OR gates 079 and 078 respectively, exactly as in the earlier machine. It should be noted that OR gate 043 inhibits the generation of MAD4 if there is a carry overflow condition. This precludes any possible interaction between an add cycle and a carry overflow condition.

9. STEP TO PS5

The machine will stay in PS4 until the D Counter is incremented to zero. To keep the machine in PS4, MAIM3 is an input to OR gate 024. This inhibits incrementing the Phase Counter until MAIM3 goes negative, and this will not happen until CDZ3 goes positive. Thus, the Phase Counter is locked in PS4 until the D Counter reaches zero.

Normally, nothing is done in PS5. However, if the last add cycle in PS4 yields a carry overflow the count of one will be added to R2 in PS5 instead of PS4.

10. SHIFT R1 LEFT (PS6)

In PS6, R1 must be shifted left if the Decimal Point Counter does not equal zero. OR gate 062 will have a negative output if the Decimal Point Counter is not zero in PS6 of a Multiply or a Divide. When its output is negative, M1L4 is caused to be negative and enables OR gate 097 to develop SAD9 and SDC9 each R1 time of C2 through C14. (For additional shift left information, see Topic E2) M1L4 is also an input to OR gate 059 (input to the Decimal Point Counter). In PS6 when R1 is being shifted left, all inputs to O-059 are negative, and the output is negative. When HOME1 goes positive, the output goes positive and increments the Decimal Point Counter.

Also, in PS6 MMDL3 is positive and is an input to AC AND gate 1154 (at the PC4 FF). HOME1 is the trigger input to A-1154; thus, the same HOME1 that increments the Decimal Point Counter and the Phase Counter also resets PC4 FF. This is the PS6 to PS3 jump. Note that if R1 is shifted left in PS6, the PS6 to PS3 jump MUST be done. But, if the Decimal Point Counter is already zero at the beginning of PS6, then MMDL3 and M1L4 are not developed (DSZ3 is positive at the input to 062). Thus, nothing is done in PS6, and at the end of PS6 the machine goes into PS7 instead of PS3 (MMDL3 is negative at A-1154 and inhibits resetting PC4 FF).

11. SHIFT DOWN IN PS7

In PS7 R1, R2, R3, and R4 must be shifted down. This means that the sync pulse and RS must be shifted up, and that RMD must be cleared out of the D Counter at R1 time. OR gate 308 causes SAD9 and SDC9 to be generated to shift up the sync pulse in C0 time of PS7 in a Multiply or Divide. OR gate 302 causes SAD9 and SDC9 to be developed during each RS and RMD time of PS7 in a Multiply or Divide. OR gate 303 causes CRD9 to be generated each R1 time of PS7 in a Multiply or Divide. (For more detailed information on shift down in PS7 of Multiply, see Topic E4). At the end of PS7, HOME1 steps the Phase Counter to zero, A-1104 causes the Common Function FF to be reset, and the machine comes out of the Multiply function.

12. CONCLUSION AND SUMMARY

In general, the Multiply functions of both types of EC-130 are the same. Specific operations are done in the same order. This can be verified by a comparison of the two Multiply Flow Charts. The only difference of any significance is that the add cycles are done in PS4 instead of in PS5. In the earlier machine, PS4 was a “dead time” in which nothing was done for 5 milliseconds. Now the “dead time” is in PS5. Of course some of the logic used to accomplish these similar operations is somewhat different, but if anything, the logic is simpler and easier to understand than in the earlier machine. Furthermore, some of the logic is unchanged at all thereby putting the machine in a light of familiarity.

K. DIVIDE FUNCTION

Division in the new model EC-130 is much the same as division in the earlier Model EC-130. The same operations must be done and in the same sequence.

1. DIVIDE FLOW CHART

Figure 5-9 (see Foldout Page 25) shows the Divide Flow Chart which is very similar to the Divide Flow Chart of the Four Counter machine. Note that PS1 and PS2 are identical in both machines. However, in PS3 there is a difference. In the later Model EC-130 there is no subtraction done in Step 3. Instead the first subtract is done in PS4, and each subsequent subtraction is done in PS5. Note that the operation is the same in both machines; only the phase step may be different. PS6 and PS7 are also the same in both machines. In the Division function the Entry Encoder is not used because there is a Divide FF which is controlled by the divide switch. The function begins when the Divide FF and the Common Function FF are set.

2. DECIMAL ALIGN (PS1)

The following description of the Divide function will be by Phase Counter step.

In PS1 of Divide, as in PS1 of all functions, only align shift R1 left is accomplished. In order to align it is necessary to develop MAIL3 and MIL4. The development of these two signals is controlled by OR gate 053. The signals PC41, PC21, and PC12 define PS1. ECF2 is negative because the Common Function FF is set. DSZ3 will be negative if R1 must be shifted left for alignment. If all five inputs to OR gate 053 are negative, the output will be negative. This causes MAIL3 to be positive, and causes MIL4 to be negative. MIL4 is one of four inputs to OR gate 097. The output of O-097 will be negative each R1 time C2 through C14 times. A negative at the output of O-097 causes SAD9 and SDC9 to be generated (for additional, more complete information on align shift R1 left see Topic E2).

3. CHANGE SIGN OF R1 (PS2)

In PS2 of the divide problem the same things must be done that are done in PS2 in the earlier EC-130. First, the sign of R1 is added to the sign of R2. OR gate 051 and inverter 052 are used to generate AIRX3 which inhibits the generation of CRA9 when AIRX3 is logic 1. AIRX3 is also used to reset the DPS FF and to set a count of four into the Decimal Point Counter.

4. SHIFT DOWN R1 to RMD

In addition, R1 is shifted down in PS2. To shift down R1, it is necessary to shift up the sync pulse, and all data except R1. Also, because it is necessary to clear R1 out to zero, CRD9 must be generated each R1 time to reset the RMD data out of the D Counter. If this is not done, RMD data will end up in R1 time. OR gate 306 causes SAD9 and SDC9 to be generated each R time except R1 in PS2 including R3 C0 time for the sync pulse. This results in the sync pulse and all data except R1 data being shifted up. OR gate 050 is used to clear the RMD data out of the D Counter. The output of O-050 goes negative each R1 time in PS2, and causes CRD9 to be generated each time it goes negative. Developing CRD9 in R1 time clears out the RMD data before it can be shifted into R2 time. (For more detailed information on shifting down R1 in Divide, see Topic E4.)

(NOTE: No operation is done in PS3 of Divide.)

5. SUBTRACT IN DIVIDE FUNCTION (PS4)

Everything that is done in PS3 and PS4 of Divide in the Four Counter machine is done in PS4 in the Three Counter machine. The first operation occurs at the beginning of PS4. If the Decimal Point Counter is zero, and the Decimal Point Storage FF is reset, the DPS FF will be set by AC AND gate 1133. The enable input to A-1133 is DSZ3. The AC trigger input comes from OR gate 011. The two inputs to O-011 are EMD4 and PC41. EMD4 and PC41 are both negative in PS3 of Divide so the output of O-011 is negative. PC41 goes positive at the beginning of PS4 so the output of O-011 goes positive. The positive transition will set the DPS FF if DSZ3 is also positive. When the DPS FF sets, EDPS1 transitions positive. EDPS1 is used to set the Decimal Point Counter to a count of three plus the number of the decimal position.

The first subtract cycle is also done in PS4. This subtract cycle corresponds to the subtract cycle in PS3 of the Four Counter of the EC-130. To do a subtract cycle in Division it is necessary to generate MSU3 and MSU4. OR gate 045 has four inputs. PC42 and PC21 define PS4 or PS5. EDV2 is negative in a Divide function, and ACOF1 will be negative as long as there is no overdraft. The output of O-045 will be negative when all inputs are negative and will cause MSU3 to be positive and MSU4 to be negative. MSU3 is applied as an input to OR gate 142 to enable CRD9 to be developed. Since in the subtract cycle RMD data is counted into the D Counter serially, it is necessary to reset the D Counter at the end of each RMD time. MSU4 is applied to OR gate 071 with TCX5 and TRO4. These three signals will cause the output of O-071 to be negative each RMD time C2 through C14. When the output of O-071 is negative, CRA9 will be inhibited. MSU4 is also applied as an input to OR gate 146 with TCX5, TRO4, and TB154. SDA9 will be developed when all four of these signals are negative. The logic of the remainder of the subtract cycle is identical to that in the Four Counter machine with one exception. If the subtract cycle yields an overdraft, it will be necessary to reset the D5 FF at the beginning of HOME1. In the earlier machine this was enabled by CED55, but in this machine it will be enabled by the signal MSU3.

6. STEP TO PS5

It is impossible to have more than one subtract cycle in PS4 of Divide because the Phase Counter is not inhibited from stepping to PS5. MSU3 is one input to OR gate 024 (the input to the Phase Counter). While it is true that MSU3 is positive during the subtract cycle and inhibits HOME1 from incrementing the Phase Counter, MSU3 is also applied as a DC input to AC AND gate 1171. The AC input to this gate is HOME1. When the output of A-1171 transitions positive it will set PC1 FF. This steps the Phase Counter from PS4 to PS5. However, it is now impossible to further increment the Phase Counter until MSU3 goes negative. Hence, the first subtract cycle is done in PS4 while all subsequent subtract cycles must be done in PS5.

7. INCREMENT R2 (PS5)

In PS5 the remainder of the subtract cycles are done, and for each subtract cycle completed, R2 will be incremented by one. This corresponds to the subtract cycles and the generation of the answer in PS4 of Divide in the Four Counter machine. If the subtract cycle in PS4 did not yield an overdraft, MSU3 will continue to be developed by OR gate 045 until there is an overdraft and ACOF1 goes positive to inhibit the generation of MSU3. ACOF1 is also an input to OR gate 080. This OR gate is used to generate ASA13 to increment R2 in Divide. If there was an overdraft in PS4 the Carry Overflow FF would have been set at the end of PS4, ACOF1 would be positive, and it would have inhibited incrementing R2 as well as inhibiting the generation of MSU3. However, if the subtract cycle in PS4 did not yield an overdraft, a successful subtraction was completed. Hence, each successive subtract cycle in PS5 will cause R2 to be incremented by one, whether or not the subtract cycle yields an overdraft. OR gate 080 will have a negative output in PS5 of Divide if the Carry Overflow FF is not set. PC42, PC21, and PC12 gate for PS5. TC24 gates for the least significant digit column, and TR14 gates R1 time. OR gate 080 gates for R1 time instead of R2 time because the count of one will be set into the A Counter at the end of R1 time by the CRA9 signal.

The final subtract of the subtract cycle yields an overdraft. Since the Carry FF is set in C15 time, and CRD9 is developed each R time, a 9 will be set into the D Counter with ACRY1 and CRD9. This 9 must be cleared to zero, so MSU3 and HOME1 are used as inputs to AC AND gate

1308 to reset the D5 FF. MSU3 takes the place of CED55 in the Four Counter machine.

8. RESTORE OVERDRAFT (Add in Divide)

When the final subtract cycle yields an overdraft, the Carry Overflow FF is set by HOME1. Since ACOF1 is an input to OR gate 045, MSU3 will go negative at the beginning of HOME time. But MSU3 does not go negative until after HOME1 has gone positive. Therefore, the Phase Counter cannot be incremented to PS6 by this HOME time, and the machine will stay in PS5 for one more line pass. The machine uses this additional line pass in PS5 to clear out the overdraft by adding RMD to R1 and to shift R2 left. RMD is added to R1, and R2 is shifted left in the same line pass. To add RMD to R1 it is necessary to generate MAD4. This is done with OR gate 039. OR gate 039 has two inputs. EDV2 is negative in any divide problem and ACOF2 is negative when the final subtraction yeilds an overdraft. When the output of OR gate 039 is negative MAD4 will be generated.

Also, when RMD is added to R1 in PS5, the Carry FF is again set in C15 time. If the DPS FF is set, RSL03 (OR gate 108) will be developed to enable CRD9 to be generated. When CRD9 is generated and the Carry FF is set, a 9 is put into the D Counter as before. But in this line pass, the machine is adding and shifting R2 left. A nine in the D Counter in C15 time would be shifted into R1 in PS6 to possibly give an incorrect answer. In the Four Counter EC-130, this nine was cleared out of the D Counter by having RSL05 develop CED55 to enable HOME1 to reset the D5 FF. In the new version of the machine, RSL03 resets the Carry FF so that the D Counter will be reset to zero by CRD9 in C15 time. (For additional, more detailed information about Addition see Topic F.)

9. SHIFT R2 LEFT (PS5)

To shift R2 left in PS5 of Divide it is necessary to generate SAD9 and SDC9. These two signals are caused to be generated in PS5 of Divide by OR gate 311. OR gate 311 has six inputs. EDV2 is negative in Divide, ACOF2 is negative in an overdraft condition, and DSZ3 is negative as long as the Decimal Point Counter is not zero. (If the Decimal Point Counter is zero the problem is completed and it will be unnecessary to shift R2 left any further.) TCX5 defines all C times from C2 through C15. TFE2 and TFF1 defines R2 time. Therefore, the output of OR gate 311 will be negative each R2 time, C2 through C15 time of PS5 in Divide. (For more detailed information on shifting R2 left in Divide, see Topic E2.) Please note that R2 is shifted left and RMD is added to R1 in the same line pass. There is no inter-action because the D Counter is not used in Addition.

10. OVERFLOW IN DIVIDE

An overflow in Divide is detected in PS5 in the same manner used in the Four Counter machine. If there is a digit other than zero in the D Counter when RSLO3 is developed, the D Counter will be reset to zero by CRD9, and the Overflow FF will be set by AC AND gate 1222. (For additional Shift Left Overflow information, see Topic E2.)

11. SHIFT R1 LEFT (PS6)

Machine operation in PS6 will be determined by the condition of the Decimal Point Counter. A count other than zero in the Decimal Point Counter indicates that the divide problem is not complete or decimal aligned in R2. Therefore, R1 must be shifted left, the Decimal Point Counter must be incremented, and a jump from PS6 to PS3 must be initiated. Shifting R1 left in PS6 of Divide is controlled by OR gate 062. OR gate 062 has three inputs; EMD4 is negative in Divide, PS64 is negative in PS6, and DSZ3 is negative if there is a count other than zero in the Decimal Point Counter. When the output of OR gate 062 goes negative M1L4 will be caused to go negative. M1L4 is one of four inputs to OR gate 097 which controls SAD9 and SDC9 to shift R1 left. (For more detailed information in shifting R1 left in Divide, see Topic E2.) M1L4 is also an input to OR gate 059. The output of OR gate 059 will increment the Decimal Point Counter when there is a transition from negative to positive. For this transition to occur, M1L4 must first be negative. Then the Decimal Point Counter can be incremented once at the end of each shift R1 left in Divide.

If, on the other hand, the Decimal Point Counter is already zero at the beginning of PS6, then nothing will be done in PS6 because the divide problem has been completed and is already decimal aligned in R2. In this case, shift R1 left is inhibited by the signal DSZ3 at the input to OR gate 062. This signal is positive, therefore, the output of the OR gate is positive. So MMDL3 must be negative and M1L4 must be positive. Because MMDL3 is negative AC AND gate 1154 is inhibited from resetting the PC4 FF at the end of PS6. Since the PC4 FF is not reset at the end of PS6, this means that the Phase Counter steps from PS6 to PS7, instead of jumping from PS6 to PS3.

12. SHIFT DOWN IN PS7

In PS7 of Divide, it is necessary to shift down R1, R2, R3, and R4. To do this in the Three Counter machine it is necessary, first, to shift up the sync pulse, then to shift up RS. It is also necessary to reset the D Counter to clear out the RMD data. If CRD9 is not developed, the RMD data will appear in R4 time. This is not desirable! OR gate 308 controls the shifting up of the sync pulse in PS7 of Divide. The three signals at the input of OR gate 308 gate for Multiply or Divide, PS7, and C0 time. Therefore, SAD9 and SDC9 will be generated each R time of C0 time. This results in shifting the sync pulse from R3 C0 to R4 C0. OR gate 302 controls shifting up RS in Multiply or Divide. The three signals at the input to O-302 define Multiply or Divide, PS7, and RS or RMD. Therefore, the output of O-302 will be negative each RS time, and each RMD time in PS7 Divide which causes SAD9 and SDC9 to be generated at the end of each RS and each RMD times.

Since it is necessary to reset the D Counter, OR gate 303 is used to cause CRD9 to be generated. OR gate 303 has three inputs; EMD4 is negative in Divide, PS74 is negative in PS7, and TR14 is negative each R1 time. Therefore, the output of O-303 will be negative each R1 time of PS7 of Divide, and causes CRD9 to be generated. (For additional, more detailed information on Shift Down, see Topic E4.)

At the end of PS7, HOME1 steps the Phase Counter to zero. HOME1 also resets the Common Function FF through AC AND gate 1104. This results in all appropriate flip-flops being reset and terminates the Divide function.

13. CONCLUSION AND SUMMARY

In general, the method of division in the Three Counter machine is the same as the method of division in the Four Counter machine. The same operations must be done, and they must be done in the same order. The only really significant change is that in the Three Counter machine nothing is done in PS3; instead the first subtract is done in PS4. All subsequent subtractions are done in PS5 and each subtraction done in PS5 results in a count of one being added to R2. Note the similarity to the operation of the Four Counter machine. The first subtraction (in PS4) never results in a count of one being added to R2 to develop the answer. But each subsequent subtraction (in PS5) always results in a count of one being added to R2. All other operations are the same and are done in the same Phase Counter steps. Of course the logic used to generate each of these operations is somewhat different in the two machines, but on the whole the logic used in the Three Counter machine is simpler than that used in the Four Counter machine. This should result in easier, more efficient trouble shooting.

L. DECIMAL POINT COUNTER

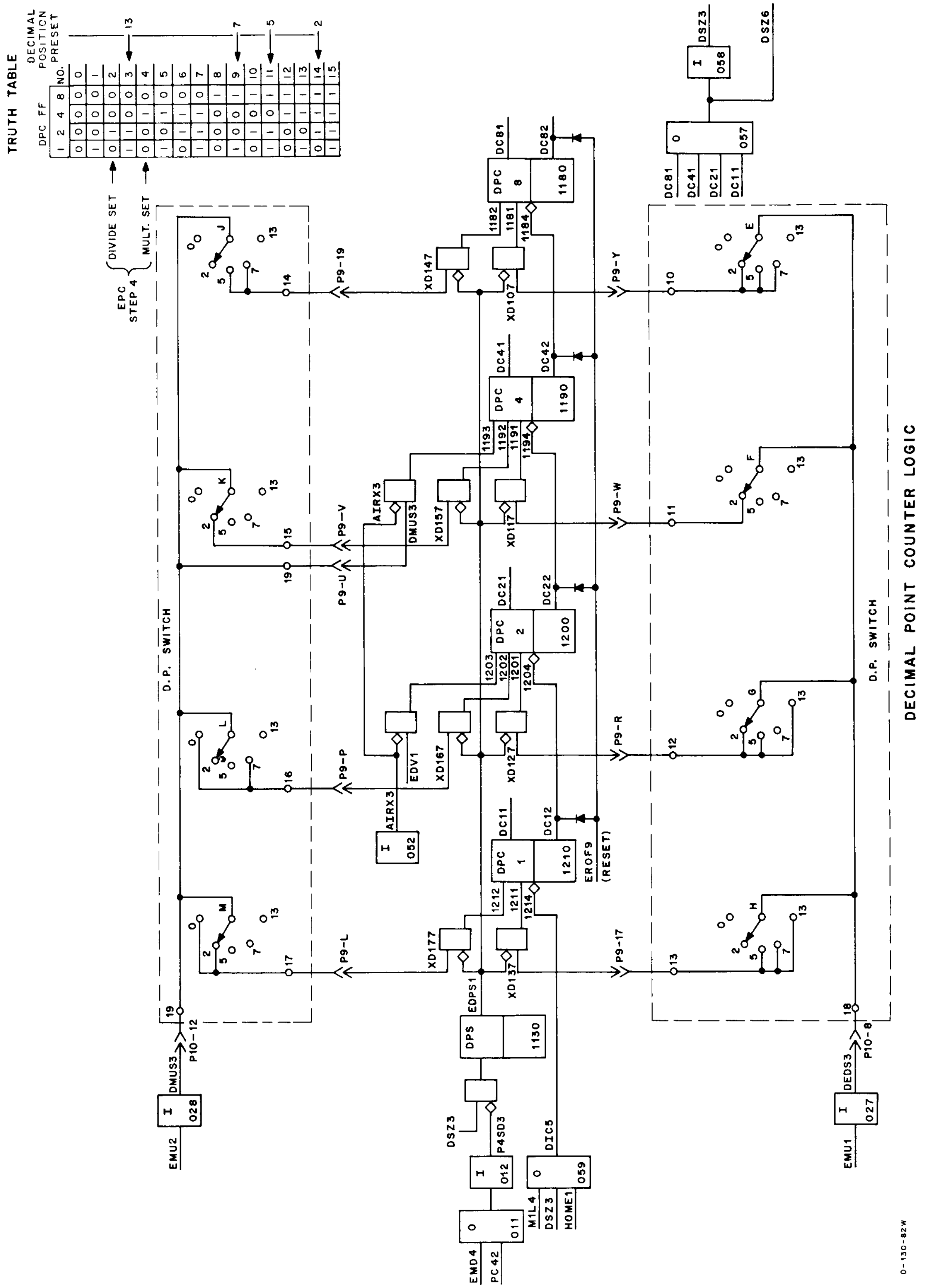
A block diagram of the Decimal Point Counter used in the Four Counter machine is shown in Figure 5-10. Its counterpart used in the Three Counter machine is shown in Figure 5-11. A brief comparison of these two block diagrams will reveal the strong similarity of the two. In Figure 5-10 the number one flip-flop can be set by AC AND gate 1212 or by AC AND gate 1211. A-1212 is gated by switch wafer M. A-1211 is gated by switch wafer H. However, in Figure 5-11 the number one flip-flop is set by AC AND gate 1211 only. Switch wafers M and H are inputs to OR gate 300 and the output of OR gate provides the DC input to A-1211. In the same fashion switch wafers L and G are inputs to OR gate 319 whose output is used to provide the DC input to A-1102 to set the number two flip-flop; switch wafers K and F are inputs to OR gate 320 and switch wafers J and E are inputs to OR gate 321 to provide the DC input to A-1181 to set the number eight flip-flop. In reality this does not change the logic of setting the Decimal Point Counter at all. It does enable the more efficient use of parts on hand to accomplish the same job. Note that there are no other changes in the Decimal Point Counter block diagrams.

M. DISPLAY

The method used to generate the complex deflection waveforms remains unchanged. However, some of the circuits used to generate the components of these complex waveforms are somewhat changed. These changes are described, circuit by circuit, as follows:

1. SEGMENT GENERATOR

The segment generator is no longer gated by the signals TCA2, TCB2, and TCC2. To take the place of these three signals, YBL5 is used. Because YBL5 is positive when it is desired to reset the segment generator, inverter 3001 is no longer needed. The new segment generator circuit is shown in Figure 5-12 with two inputs: YBL5 and YBDP3. When either of these two signals is logic one, inverter 3002 is off and has a negative (logic zero) output. This negative output keeps the segment generator reset transistor turned on to prevent the sawtooth waveform from being generated. YBDP3 is normally negative and enables YBL5 to control the segment generator. YBL5 is negative when it is desired to display a segment; hence, with both inputs to OR gate 3000 negative, inverter 3002 is turned on. With inverter 3002 turned on, the segment generator reset transistor is turned off, thus allowing a sawtooth to be developed. (An interesting result of using YBL5 is that no sawtooth waveform is generated unless that segment is actually intensified.)

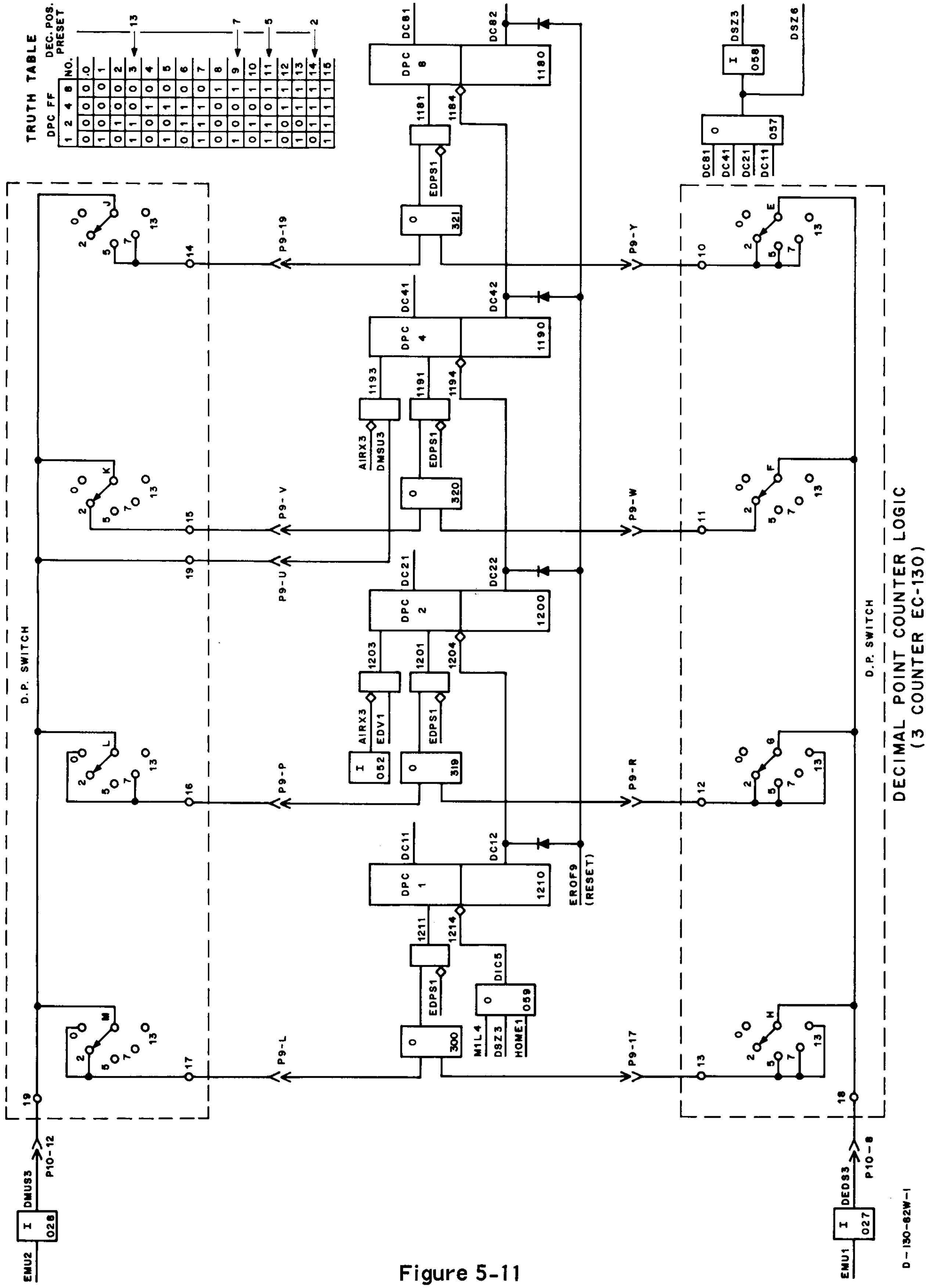


TRUTH TABLE

NO.	DPC FF 1	DPC FF 2	DPC FF 4	DPC FF 8	DECIMAL POSITION PRESET
0	0	0	0	0	
1	1	0	0	0	
2	0	1	0	0	
3	1	1	0	0	13
4	0	0	1	0	
5	1	0	1	0	
6	0	1	1	0	
7	1	1	1	0	
8	0	0	0	1	
9	1	0	0	1	7
10	0	1	0	1	
11	1	1	0	1	5
12	0	0	1	1	
13	1	0	1	1	
14	0	1	1	1	2
15	1	1	1	1	

EPC STEP 4 { DIVIDE SET, MULT. SET }

Figure 5-10



TRUTH TABLE

NO.	DPC FF 8	DPC FF 4	DPC FF 2	DPC FF 1	DEC. POS. PRESET
.0	0	0	0	0	
1	0	0	0	1	
2	0	0	1	0	
3	0	0	1	1	13
4	0	1	0	0	
5	0	1	0	1	
6	0	1	1	0	
7	0	1	1	1	
8	1	0	0	0	
9	1	0	0	1	7
10	1	0	1	0	
11	1	0	1	1	5
12	1	1	0	0	
13	1	1	0	1	
14	1	1	1	0	2
15	1	1	1	1	

Figure 5-11

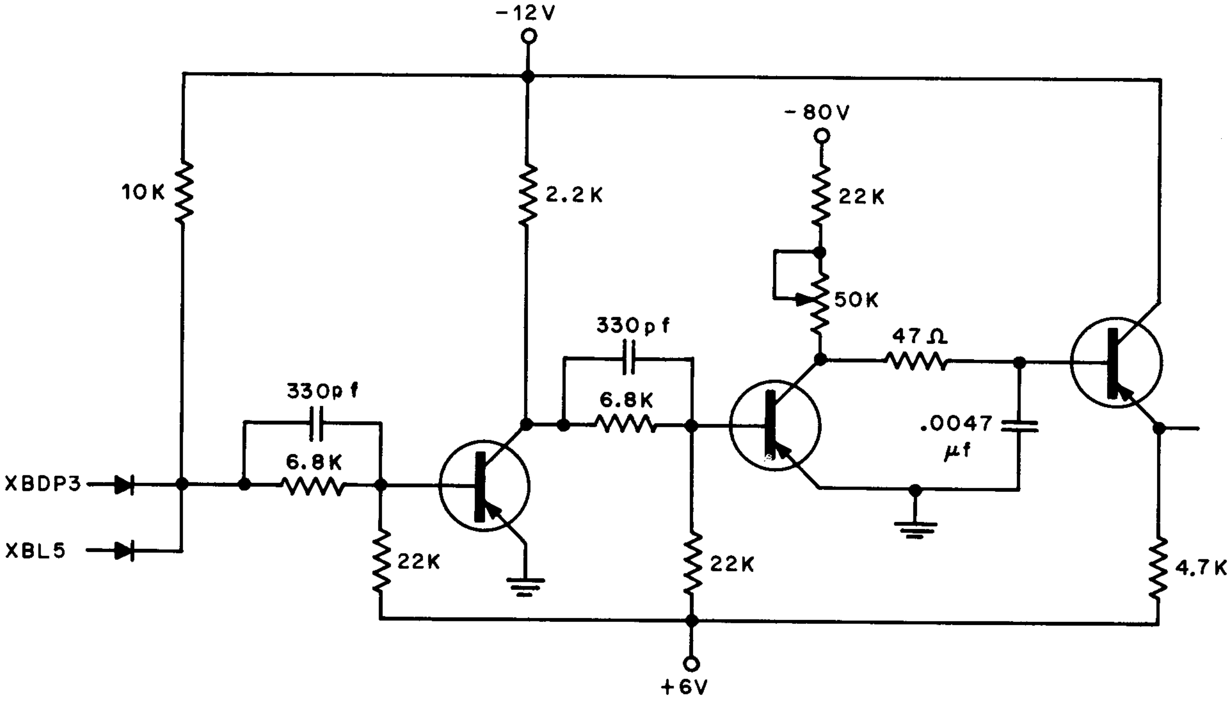


Figure 5-12

In addition to the logic change as described, there are two circuit changes. In the segment generator of the Four Counter machine there is a 47 ohm resistor connected between the .0047 μf capacitor and ground. In the new EC-130 this 47 ohm resistor is connected between the .0047 μf capacitor and the collector of the segment generator reset transistor. It serves the same purpose as before; that is, it limits collector current when the reset transistor is turned on. This protects the transistor from thermal damage. The second circuit change is that there is no longer a clamp diode connected from the .0047 μf capacitor to -12 volts. Recall that it is necessary to clamp the capacitor to some maximum negative value. If this were not done, and the reset transistor failed for some reason to turn on, the capacitor would charge to -80 volts, exceeding the maximum collector voltage and base voltage rating of all the associated transistors. It is now realized, however, that the capacitor is clamped to a maximum of -12 volts even without the clamp diode. If the voltage on the capacitor exceeds -12.1 volts, the collector-base junction of the emitter follower is forward biased and clamps the capacitor to a maximum of about -12.1 volts.

2. SEGMENT SWITCHES

The Segment Switches have also been changed (see Figure 5-13). This circuit is simpler than the earlier version. The sawtooth waveform is applied to a voltage divider comprised of two 4.64K 1% resistors in series. The other end of the voltage divider is connected to the appropriate Dot Generator. The collector of a transistor is connected between the two 4.64K resistors. When the transistor is turned off, current from the Segment Generator develops a sawtooth voltage waveform across the 500 ohm potentiometer (character width or height adjustment). But when the transistor is turned on, all this current is shorted to ground through the transistor, and no sawtooth voltage is developed across the 500 ohm potentiometer. Note that the base bias circuitry is the same as in the earlier EC-130, and that both the Vertical and Horizontal Segment switches are identical.

3. HORIZONTAL STAIRCASE GENERATOR

The Horizontal Staircase Generator is changed only slightly. (See Figure 5-14.) In the Four Counter machine, YYC1 and YCPR3 are inputs to OR gate 3006 to reset the staircase generator. But, in the new machine, YCPR3 is not generated, so TFG2 is used instead. The result is the same as before. YYC1 will go negative in C15 time, and TFG2 will go negative at the end of R4 C15 time. When both signals are negative, inverter 3007 is turned on to reset the generator.

Second, the clamp diode has been removed from the .47 μf capacitor to -12 volts for the same

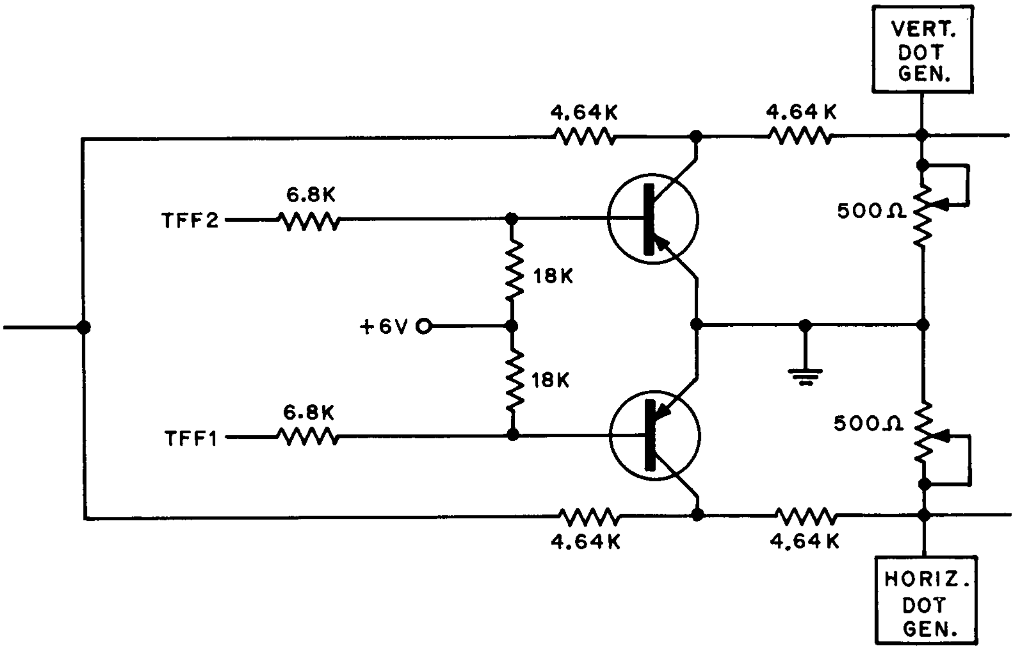


Figure 5-13

reason as listed in the Segment Generator description. The capacitor is clamped through the collector base junction of the first emitter follower. The Horizontal Staircase Generator circuit is shown in Figure 5-14.

The third change was made to reduce the possibility of a wavering display. The load resistor of OR gate 3004 is reduced to 12K and is returned to -8V. This necessitates a change in the size of the capacitor in the base of the step control transistor. It is now .0022 μf.

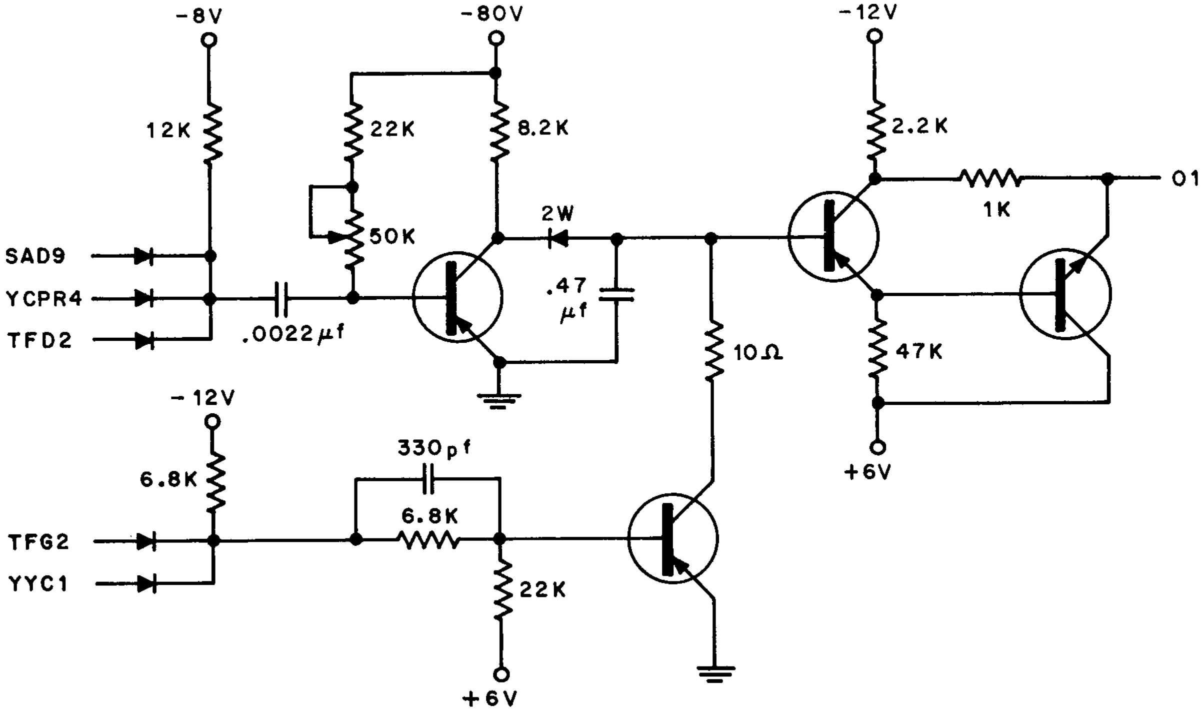


Figure 5-14

4. COMPARE AND INTENSIFICATION

The Compare logic involves only three small changes. First, PSZ3 is no longer an input to AND gate 225, so YCPR4 is developed even in a function or digit entry.

Second, YCPR3 is no longer developed. Hence, inverter 227 doesn't exist. Third, to generate SAD9 for display, OR gate 031 is used. O-031 has four inputs. PC41, PC21, and PC11 define PSZ so that the only time the output of O-031 can go negative is when there is a compare in PSZ. When the output does go negative SAD9 is caused to be developed.

In the blanking circuitry, PSZ3 is no longer an input to AND gate 250 because PSZ3 is no longer developed. Instead, ECFD4 is used to inhibit unblanking during a function or digit entry. OR gate 199 is used to inhibit unblanking during the last three microseconds of a segment. By applying the output of O-199 as an input to A-250, inverter 200 is no longer needed or used.

TC153 can no longer be used to enable the Display Control FF to be reset, because TC153 no longer exists, so TCX5 is used, and there is no change in timing.

DIVIDE FLOW CHART (3 COUNTER EC-130)

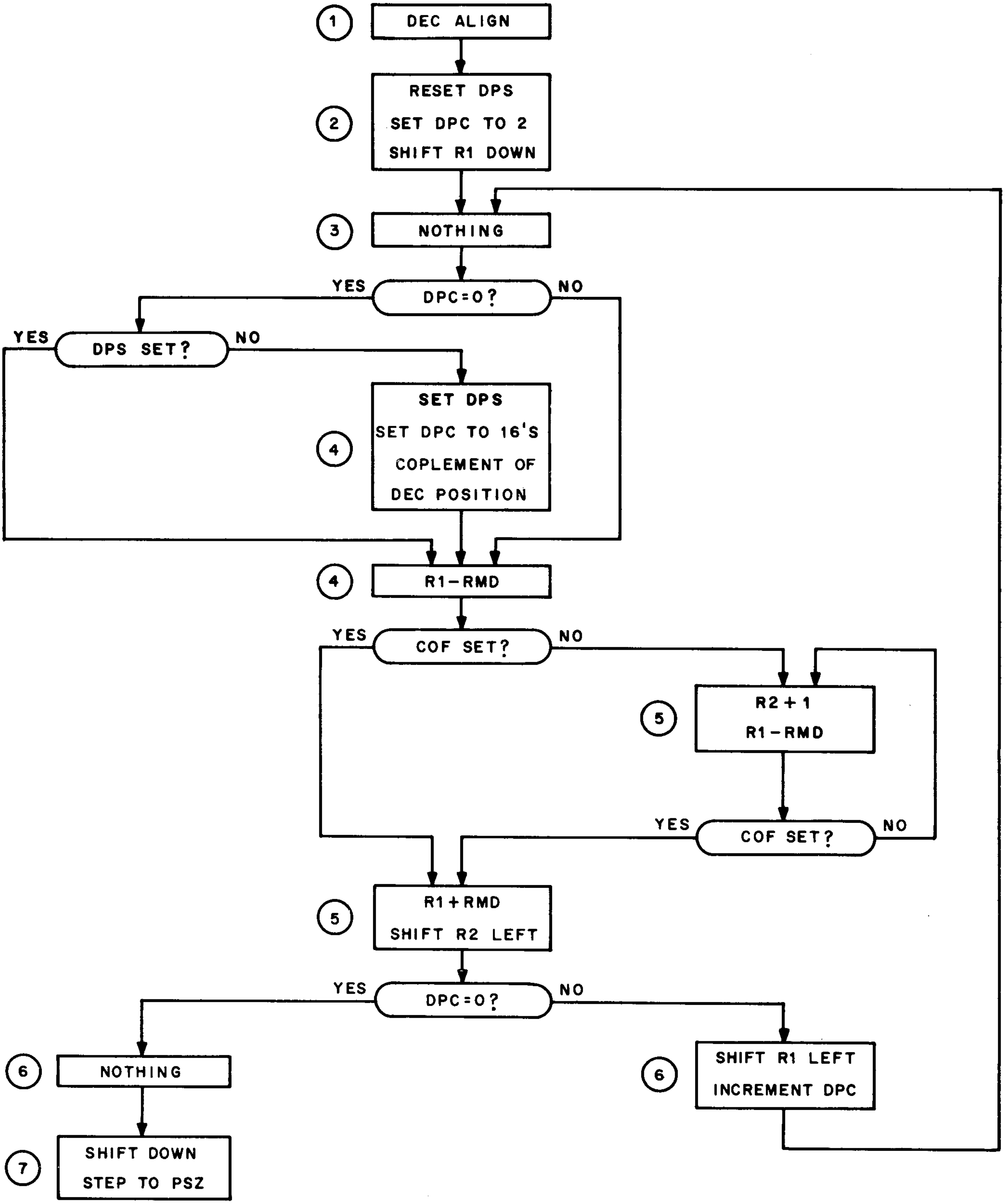


Figure 5-9

MULTIPLY FLOW CHART (3 COUNTER EC-130)

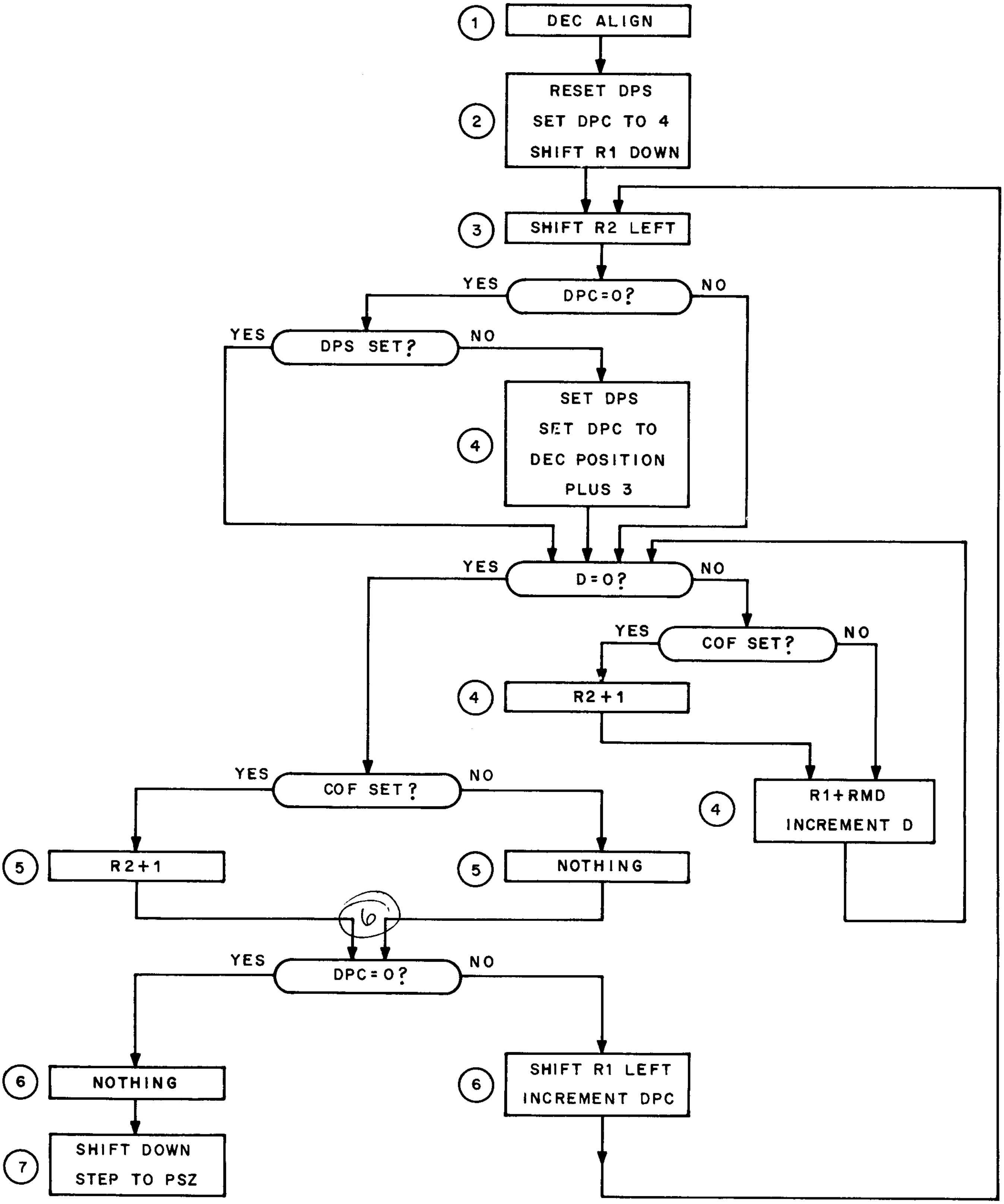


Figure 5-8